JEITA EDA -WG Activity and Study of Interconnect Model
Part-2

March 10, 2006
European IBIS SUMMIT in Munich

JEITA EDA-WG
Takeshi Watanabe (NEC Electronics)
Atsuji Ito (Panasonic)
Kazuhiko Kusunoki (KAW/Keihin Artwork)

JEITA ; Japan Electronics and Information Technology Industries Association

© JEITA 2006. All Rights Reserved.
Outlines

1. JEITA EDA-WG Activities
2. Short Term Direction of JEITA EDA WG
3. Study of Interconnect Model
4. JEITA IBIS Model Portal site
5. Progress Report
1. JEITA EDA-WG Activities

Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics
Cellular Phone, LCD /PDP TV,
Digital Camera/Video, DVD Recorder
(Digital, RF, and Analog circuits)

Auto Mobile Electronics?
(Motor Drive, EMC)

< Applicability of IBIS V4.1 >

© JEITA 2006 All Rights Reserved.
EMI, SI and PI for Digital Consumer Electronics

<Background>

EMI  High-speed Clock Frequency
SI   DDR, PCI, PCI-Express
PI   High density and Large scale IC

SiP and Module, PCB level

EMI, SI and PI Simulation Technology
EDA Model for EMI, SI and PI Simulation

- PCB
- FPC
- RF Modules
- LSI Model
  - IC Chip
  - IC Package
- Passive Component (LCR, Filter)
- Display device
- Discreet Semicon
- Crystal Oscillator
- Connectors
- Cables
Focus of EDA Model for Simulation

9 components

ICs
RF Modules
Passive Components (LCR, Filter)
IC Package
EDA Models For Digital Consumer electronics
Crystal Oscillator
Connectors
Cables
PCB
FPC

© JEITA 2006. All Rights Reserved.
JEITA EDA-WG Member

15 Major Companies

Digital Consumer Electronics Supplier

EDA (internal/vendor)

EDA Models For Digital Consumer electronics

Semicon

NECEL Toshiba

Passive Components

TDK Murata

PCB

Connectors

JAE

Panasonic

Sony

Sharp

Canon

Toshiba

Fujitsu

Mitsubishi

Cadence Japan

© JEITA 2006. All Rights Reserved.
2. Short Term Direction of JEITA EDA WG

• Study of Interconnect Model
• IBIS Models of Passive Components and Connector and other Components
• JEITA IBIS Model HP
• Discussion about Case study of Simulation for Digital Consumer Electronics and JEITA-IBIS Joint meeting include European IBIS member periodically
3. Study of Interconnect Model

SI Model (Connector, PCB, Cable)

Signal
InfiniBand
RapidIO
DDR
PCI-Express

Waveform measurement point

Connector

 Terminator

Passive Component

Cable, FPC

JAE (Japan Aviation Electronics Industry)
FI-X Series

© JEITA 2006. All Rights Reserved.
Study of Interconnect Model for Signal Integrity

◆ Target Application; DDR, PCI-Express etc.
◆ EDA Model; Connectors, Passive Components, PCB (Via, Pattern), (LSI)
◆ Simulation Tool; Cadence etc.
SI Model  (Connector- Type B; stacked module, PCB, Cable)

Signal
PCI-Express
HyperTransport

Waveform measurement point

Signal Generator

Connector

SMA Connector

WB3 Series

© JEITA 2006. All Rights Reserved.
SI Model (Connector- Type C, PCB, Cable)

Signal
PCI-Express
HyperTransport

Connector

Waveform measurement point

SMA Connector

Signal Generator

© JEITA 2006. All Rights Reserved.
SI Model (Connector, PCB, Cable, LVDS)

Waveform measurement point

LVDS
Connector
LVDS
Terminator

Signal Generator
SMA Connector
Cable, FPC

© JEITA 2006. All Rights Reserved.
Simulation Model

Equivalent circuit

Simulation

TML

Measurement

© JEITA 2006. All Rights Reserved.
Evaluation Board

Connector

Fi-X Connector

SMA Connector

SMAR006D00

Spacer

© JEITA 2006. All Rights Reserved.
layer structure

SMA Connector

Spacer

© JEITA 2006. All Rights Reserved.
All Component
(TML, Passive Components, VIA, Connector)
4. JEITA IBIS Model Portal site Plan

Library

Verification TOOLS

NG IBIS

IBIS Model

IBIS COOK BOOK

SI and EMI Simulation

E-Learning

instruction manual

Library

© JEITA 2006. All Rights Reserved.
JEITA IBIS Model Portal Site Contents

- IBIS Documentations
  COOK BOOK
- IBIS Library
  Instruction manual
  IBIS Model Storage rack
- IBIS Training / IBIS E-Learning
- IBIS Free Tool

Support for IBIS Users
IBIS Indicator™ The IBIS Model Engineering Stationery
By KAW/JAPAN  www.kaw.co.jp

Indicate IBIS

Output Current

Reference Voltage

Rise/Fall Speed

Validate IBIS

Error

Warning

IBIS Model Engineering Stationery

Before

Automatic Correction

After

Correction IBIS

Indicate Signal Wave

© JEITA 2006. All Rights Reserved.
5. JEITA EDA-WG Progress Report

- Study of Interconnect Model
- IBIS Documentations
- IBIS Free Tool

~March of 2006
Evaluation for using different kind of model.

Which model might be better to practical use for every simulation engineer.

- Murata Filter
- TDK Filter
- JAE Connector

S-parameter?  Spice?  RLGCC?  ?
Compare Measurement with Simulation

Measurement  Simulation

MHz~GHz

Model

S-para  Spice  RLGc

Ω/H/S/F

© JEITA 2006. All Rights Reserved.
Testing the VIA effect

© JEITA 2006. All Rights Reserved.
IBIS Documentations

IBIS Cook Book in Japanese

Translation by JEITA EDA-WG members

Coming Soon
Spricht hier jemand Japanisch?

© JEITA 2006. All Rights Reserved.
Convergence analysis

Clamp double-counting

Finding Irregular point

20 Check Items

With the exception of Syntax
**IBISIndicator™**

- **Compare Check IBIS** which are same Output current in the data sheets.
- **Check and Auto-fix** for IBIS Non-monotonic error.
- **Find the problems** of IBIS which has no-error in IBIS Syntax check.

© JEITA 2006. All Rights Reserved.
IBIS Free Tool

IBISIndicator™ The IBIS Model
Limited Edition

Engineering Stationery

Menus in English

Reference Voltage

Output Current

Rise/Fall Speed

Now Available for Free

And More Functions

Download: www.edaconnect.co.jp

© JEITA 2006. All Rights Reserved.
We hope to discuss case study of IBIS with European IBIS members periodically.

Thank you for all the help EIA/IBIS Committee!

Auf Wiedersehen!