driver schedules: pre-/de-emphasis and frequency/data-rate issues

Eckhard Lenski
DATE, Munich, Germany
14th March 2008
driver schedule: pre-/de-emphasis and frequency/data-rate issues

summary

Pre-/De-emphasis basics

examples

Frequency /data rate

Driver schedule retrospection
Pre-/De-emphasis basics

driver schedule: pre-/de-emphasis and frequency/data-rate issues

Examples

Frequency/data rate

Driver schedule retrospections

summary
Pre- or DE-emphasis is often realized with current-mode-drivers and you can define 4 states:

- Low
- Low-Pre
- High
- High-Pre

Each bit after a change of the logic state is emphasized.
pre-emphasis switching modi

There exist 4 possible switching modi

1. Low-Pre $\rightarrow$ High-Pre $\ldots$ 10 $\rightarrow$ 1
2. Low $\rightarrow$ High Pre $\ldots$ 00 $\rightarrow$ 1
3. High-Pre $\rightarrow$ Low-Pre $\ldots$ 01 $\rightarrow$ 0
4. High $\rightarrow$ Low-Pre $\ldots$ 11 $\rightarrow$ 0
Driver schedule retrospections

Pre-/De-emphasis

Summary

Examples

Frequency/data rate

driver schedule: pre-/de-emphasis and frequency/data-rate issues
driver schedule information

- IBIS summit presentations
  - Arpad Muranyi
  - Bob Ross
  - Chris Reid
  - Hazem Hegazy
  - Lance Wang
  - .......

- IBIS cookbook 4.0

- IBIS spec 4.2

- ????
driver schedule static curves

[Model] 2-Driver-schedule

[Voltage Range] 3.30V 3.1350V 3.4650V

[GND Clamp]

[POWER Clamp]

[Pulldown]

[Pullup]

[Driver Schedule]

MODEL_1 0s NA 0ns NA
MODEL_2 0.5ns NA 0ns NA

[Model] Model_1

[GND Clamp]

[POWER Clamp]

[Model] Model_2

[GND Clamp]

[POWER Clamp]

[Pulldown]

[Pullup]
driver schedule: pre-/de-emphasis and frequency/data-rate issues

Pre-/De-emphasis

Examples

Driver schedule retrospections

Frequency / data rate

summary
Data signal & clock signal

Data signal1 (NRZ)

Data signal2 (NRZ)

Data sampling window

Bit time or UI

Clock signal

Clock period

11 © Nokia Siemens Networks driver schedule: pre-/de-emphasis and frequency/data rate issues Lenski / 14th March 2008
Correlation
- Between Unit Intervall and Data rate
- Data rate = 1 / UI
  - e.g.
  - 1.25Gbps = 1 / 800e-12s
- It takes one UI for one bit to be transmitted

Assuming a 1010.. Pattern
- For binary data signals:
  Frequency = data rate /2
- This is not the clock frequency
- Eg.:
  - Datarate → Frequency
  - 5Gbps → 2.5GHz
  - 1.25Gbps → 625MHz
different patterns

10101010

11001100

11101100
**classic IBIS model**

Normally the rising and falling times of the IBIS model determines the max. frequency where the model can be used.

**Rule of thumb:** $F_{\text{max}} \text{ IBIS model} = \frac{1}{(\text{trise} + \text{tfall})}$

**Eg.:** IBIS model with trise 2ns, tfall 2ns

$F_{\text{max}} = \frac{1}{4\text{ns}} = 250\text{Mhz}$
driver schedule for Multi-Gigabit applications

Old rule of thumb: Fmax IBIS model = 1/ ( trise + tfall )
This rule is no longer valid

The signal needs to be
**long enough** above high threshold
Or
**Long enough** below low threshold
And this for many times
Examples

Summary

Driver schedule: pre-/de-emphasis and frequency/data-rate issues

Pre-/De-emphasis

Driver schedule retrospections

Frequency/data rate

Examples

Summary

Driver schedule: pre-/de-emphasis and frequency/data-rate issues

Pre-/De-emphasis

Driver schedule retrospections

Frequency/data rate
low frequencies pushpull-cmos model

Model has got risetime and falltime of about 1ns
So it could be used up to 500MHz
High frequencies pushpull-cmos model

Above 500MHz:
The behavior looks suspicious

Frequency / data rate
Signal characteristics for pre-emphasis

- Each bit after a change of the logic state is 'emphasized'.
- Rising edge contains information for the data pattern 1 1.
- Falling edge contains information for the data pattern 0 0.
**driver schedule @ 250MHz (tp=4ns)**

- **Rising part finished,**
  - Model stays in this logic HIGH state,
  - until "tool" switches to LOW

- **Rising edge part of driver schedule**
Model shows the pre-emphasis behavior, because the pattern 11 and 00 can be fulfilled.

Rising part finished, And the „tool“ switches to LOW

Rising edge part of driver schedule
Model shows correct pre-emphasis behavior for the first bit, but for the second bit, it is switched off.
driver schedule @ 1000MHz (tp=1ns)

Model shows a switching from High to Low, but between High-Pre and Low-Pre, So only the pattern 101010 will be shown correctly
There is not enough time for the first bit
Because the tool starts switching off
eye diagrams preliminary

!! Under construction !!
driver schedule @ (250MHz)  UI = 2000ps
driver schedule @ (500MHz)  UI = 1000ps
driver schedule @ (750MHz) UI = 666.66ps
driver schedule @ (1000MHz) UI = 500ps
summary

driver schedule:
pre-/de-emphasis and
frequency/data-rate
issues

Pre-/De-emphasis

Examples

Driver schedule retrospections

Frequency/data rate
scope of application

• For normal pushpull-cmos

- 0 Fmax frequency

• For Driver schedule modeling pre-emphasis

- 1.25Gbps
- 2.5Gbps
- 3.125Gbps
encoded pattern

• For normal cmos
  – 10 pattern is encoded in the model

• For Driver schedule modeling pre-emphasis
  – 1100 pattern is encoded in the model
Summary

• Ibis models (exception of driver schedule) are ’valid‘ for a frequency range which is set by the risefalltime of the model

• Driver schedule modeling pre-emphasis are valid only for one datarate/frequency, corresponding to the UI they are made for

• Tool don‘t cares about encoded bitpattern in model or the included bit-time / UI

• User has to take care that the „frequency“ corresponds to UI
Thank You

• Questions?