Macromodels of IC Buffers Allowing for Large Power Supply Fluctuations

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Introduction

Models of IC buffers required for the system-level assessment of signal integrity and EMC effects via numerical simulation

Include the effects of power supply variations

- Recent applications (e.g., stacked SiP devices, memories) exhibit large variation (30÷40%)
- State-of-the art models allow only for limited variations (10÷15% of the nominal power supply voltage)

Improve existing models
Example

Waveform distortion produced by the state-of-the-art models

Where do these differences come from?

**Mπlog model structure**

- **e.g., IC output buffer** (single-ended)

- **2-piece model representation**
  \[ i(t) = w_H(v,vdd,t) \cdot i_H(v,vdd,d/dt) + w_L(v,vdd,t) \cdot i_L(v,vdd,d/t) \]

- **Underlying (simplifying) assumptions**
  
  Model parameters computed for the **nominal power supply VDD**

  Weighting signals → \( w_{H,L}(t) \)
  Submodels \( i_{H,L} \) → \( i_H = i_H(vdd-v,d/dt), i_L = i_L(v,d/dt) \)
Mπlog model structure, cont’d

- Ideal power supply @ 70% VDD

Graph showing voltage over time with labels for reference and Mπlog model.
A – static compensation

Static surface for vdd ∈ [70,130]%VDD

- State-of-the-art: \( i_L(v, VDD) \) (—)
- Complete 2D surface (model complexity increases)
  - \( i_L(v, vdd) = k_L(vdd) \times i_L(v, VDD) \) [2]

A – static compensation, cont’d

- Static surface for vdd ∈ [70, 130] % VDD

- Actual i-v operating region

- Proposed model

\[ i_L(v, vdd) = k_L(vdd) \times i_L(v, VDD) \]

computed along the TL load lines
A – static compensation, cont’d

\[ i_L(v,v_{dd}) = k_L(v_{dd}) \times i_L(v,V_{DD}) \]

- include the information of the analytical MOS equations
- triode region [3]

\[ i_D \approx A_n (V_{GS} V_{DS} - V_{DS}^2/2) \]

- \( A_n \) fitted with \( i_L(v,V_{DD}) \)
- \( k_L(v_{dd}) \) by matching analytical NMOS equation with model equation along the load lines

- Need of static characteristics @ VDD only (—)

A – static compensation, cont’d

DC model response

Relative errors less than 2%

Possible discrepancies outside the operating region do not affect model accuracy

- reference
- enhanced model (static comp.)
A – static compensation, cont’d

- Ideal power supply @ 70% VDD

- Accurate prediction even with a very simple approximation of the 2D static surface
B – delay compensation

Embed the $\tau$ (UP,DOWN) information in the model

$$w_{H,L}(t) \to w_{H,L}(t - \tau(vdd))$$
B – delay compensation, cont’d

☐ Delay propagation [3]

\[ \tau_P(vdd) \cong \tau_P(VDD) \times (VDD/vdd) \quad (\text{accuracy: } \sim 5\%) \]

\[ w_{H,L}(t) = w_{H,L}(t - \tau(vdd)) \]
\[ \tau(vdd) = \tau_P(VDD) - \tau_P(vdd) = \tau_P(1-VDD/vdd) \]


No additional information is required
Enhanced model performance

- Ideal power supply @ 70% VDD

![Graph showing voltage over time for reference and enhanced models with 70% VDD.]

- Same results for 130% VDD

Good accuracy
Enhanced model performance, cont’d

Realistic test

Accuracy confirmed for $v_{dd}(t) > 40\% VDD$
Current vs. enhanced models

\[ i(t) = w_H(v,v_{dd},t) \cdot i_H(v,v_{dd},d/dt) + w_L(v,v_{dd},t) \cdot i_L(v,v_{dd},d/t) \]

<table>
<thead>
<tr>
<th>Model</th>
<th>Submodels ( i_{H,L} )</th>
<th>Weighting signals ( w_{H,L} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M(\pi)log</td>
<td>( i_{H,L}(v,VDD,d/dt) )</td>
<td>( w_{H,L}(t) )</td>
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<tr>
<td>Enhanced M(\pi)log</td>
<td>( i_{H,L}(v,v_{dd},d/dt) )</td>
<td>( w_{H,L}(t-\tau(v_{dd})) )</td>
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- no additional characterization required
- same complexity → same speed-up (10 ÷ 100x)
Conclusions

- Generation of enhanced device models for large VDD variations (>30%)
- Simplified analytical equations for static & delay compensation
- High accuracy verified on realistic tests
- Apply to different device types (e.g., precomp)
MOCHA, MOdelling and CHAracterization for SiP - Signal and Power Integrity Analysis

  “Develop reliable modelling and simulation solutions for SiP design verification”

- Participants:
  - STMicroelectronics M6 SRL (Italy)
  - Politecnico di Torino (Italy)
  - Cadence Design Systems GmbH (Germany)
  - Agilent Technologies (Belgium)
  - Universidade de Aveiro (Portugal)
  - Microwave Characterization Center (France)

- Work Packages
  - IC power integrity model
  - IC buffers’ innovative modelling approach
  - SiP design and verification EDA platform
  - SiP signal integrity measurement platform
Q&A