Enhanced $\mathcal{M}\pi\log$ Models for Power Integrity Analysis.
Modeling from simulation and measurement, IBIS data extraction, crossvalidation

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MOCHA, MOdelling and CHAracterization for SiP - Signal and Power Integrity Analysis

(www.mocha.polito.it)

  “Develop reliable modelling and simulation solutions for SiP design verification”

- Participants:
  - Numonyx Italy Srl (Italy) [Coordinator]
  - Politecnico di Torino (Italy)
  - Cadence Design Systems GmbH (Germany)
  - Agilent Technologies (Belgium)
  - Universidade de Aveiro (Portugal),
  - Microwave Characterization Center (France)

- Work Packages
  - WP1, IC power integrity model
  - WP2, IC buffers’ innovative modelling approach
  - WP3, SiP design and verification EDA platform
  - WP4, SiP signal integrity measurement platform

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WP2 overview

Objective: Development of accurate and efficient models of digital ICs

- Overcome current limitations of existing models
  
  e.g., state-of-the-art models allow only for limited power supply variations

- Generate models from measurements & simulations
WP2 achievements (i)

- Availability of the General structure of the extended model for digital buffers
- Procedure for parameter estimation from simulation / measurement
- Model implementation in different formats (HSPICE, ELDO, VERILOG-A,...)
- Application to test cases (proprietary and third party devices) from simulation
WP2 achievements (ii)

Model Accuracy, second test case *(estimation from simulation)*

<table>
<thead>
<tr>
<th></th>
<th>Eye opening</th>
<th>Error</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference (trans. level)</td>
<td>72%</td>
<td>-</td>
<td>773 s</td>
</tr>
<tr>
<td>IBIS</td>
<td>78.8 %</td>
<td>9.5 %</td>
<td>13 s</td>
</tr>
<tr>
<td>Proposed (MπLOG)</td>
<td>73.8 %</td>
<td>2.5 %</td>
<td>31 s</td>
</tr>
</tbody>
</table>

- Improved Accuracy
- High efficiency
WP2 achievements (iii)

- Design two test boards for the characterization of the IC ports of the MOCHA test cases
  
  e.g., first test case, DQ0 I/O buffer

Device models from transient port voltage and current responses recorded during IC normal operation
WP2 achievements (iv)

- **Tool** for the interactive generation of IC models

→ **Mπlog** ver. 5.3, available at www.emc.polito.it

Guided step-by-step modeling procedure
WP2 achievements (v)

- procedure for the extraction of device characteristics suggested by IBIS from the estimated models
X-Validation (i)

Test case: 512Mb LPDDR third party device, in 70nm technology and clock frequency of 133MHz.

Models:

- Reference Transistor-level
- IBIS
- MPLOG (from simulation)
- MPLOG (from measurements)

<table>
<thead>
<tr>
<th></th>
<th>IBIS</th>
<th>MPLOG (sim)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_COMP</td>
<td>3.1pF</td>
<td>3.045 pF</td>
</tr>
</tbody>
</table>
X-validation (ii)

[Diagram with two graphs:

1. Pulldown graph:
   - X-axis: Voltage (V)
   - Y-axis: Current (mA)
   - Lines: Reference (dashed), MPILOG (sim) (dotted), IBIS (circles)

2. Pullup graph:
   - X-axis: Voltage (VCC-V)
   - Y-axis: Current (mA)
   - Lines: Reference (dashed), MPILOG (sim) (dotted), IBIS (circles)
X-validation (iii)

[GND Clamp]

[POWER Clamp]
X-validation (iv)

[Rising waveform]

[Reference]

[MPILOG (sim)]

[IBIS]

[Falling waveform]
X-validation (v)

...model from real measured data
X-validation (vi)

...model from real measured data

[Rising waveform]

V = \begin{cases} 
\text{IBIS (typ)} & \\
\text{IBIS (min)} & \\
\text{IBIS (max)} & \\
\text{Measurements} & \\
\text{MPILOG (meas)} & 
\end{cases}

R_{\text{fixture}} = 47 \ \Omega \\
L_{\text{fixture}} = 18 \ \text{nH} \\
C_{\text{fixture}} = 7.4 \ \text{pF} \\
V_{\text{fixture}} = 0\text{V}
Q&A