Physics and Modeling of Vias in Printed Circuit Boards

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(1) The Problem with Vias
(2) Physics of Vias
(3) Models for Vias
(4) Application Example
(5) Conclusions
(2)

The Problem with Vias
The Problem with Vias …
The Problem with Vias …

Signal Integrity Problems:
Attenuation, Reflection, Dispersion, Interference, Crosstalk
The Problem with Vias …

Power Integrity Problems:
Voltage Drop, Switching Noise, Crosstalk
The Problem with Vias …

Electromagnetic Compatibility Problems:

Near Field Coupling, Radiated Emissions
(2)

Physics of Vias
Currents on Via Structures

Via (Signal) Current
Conduction Return Current
Displacement Return Current

Figures by R. Rimolo-Donadio
Electric Fields Between Plates

Figures by R. Rimolo-Donadio

Excitation: Gaussian pulse ($f_{\text{max}} = 40$ GHz)
Electric Fields Between Plates

Top View, 5th cavity

Finite Planes

Top View, 5th Cavity

Infinite Planes

Figures by R. Rimolo-Donadio
Influence of Ground Vias

1 Ground Via:

![Image of a ground via with labels](image-url)
Influence of Ground Vias

2 Ground Vias:
Influence of Ground Vias

4 Ground Vias:
Influence of Ground Vias

6 Ground Vias:
Influence of Ground Vias

**Graph:**
- **X-axis:** Frequency [GHz]
- **Y-axis:** Magnitude of $S_{12}$ [dB]

- **Legend:**
  - 1 GND vias: Blue dotted line
  - 2 GND vias: Red dashed line
  - 4 GND vias: Green dot-dashed line
  - 6 GND vias: Black solid line
Influence of Ground Vias

Effect of location of ground vias:

- No GND Vias
- 4 GND Vias, s=160 mil
- 4 GND Vias, s=80 mil
- 4 GND Vias, s=40 mil
Physics of Vias – Summary

- Vias „live“ within a parallel plate environment
- Shape and size of the plates have an impact
- Ground vias can be used to control that impact
- Return currents are a mixture of displacement and conduction currents
(3)

Models for Vias
PCB Teardown

Signal and Power Vias

Power Planes

Planar Circuit Models

Stripline

Transmission Line Models

Picture courtesy IBM Yorktown (Y. Kwark)
A “Physics-Based” Model for Vias
A “Physics-Based” Model for Vias

Simple example:

Port 1

Port 2

$\varepsilon_r = 4.4$
$tan\delta = 0.02$

360x360 mil

PMC

Via centered:
Radius 5mil
Antipad 10mil

~60 fF

~60 fF

$Z_{pp}$

$C$

Port 1

Port 2

20\log|Z_{pp}| [dB-Ohm]

frequency [GHz]

~60 fF

~60 fF
Planar Circuit Model I

**CRM**

Port i \((x_i, y_i)\)

Port j \((x_j, y_j)\)

Open Plane Edges

\((0,0,0)\)

\((a,0,0)\)

\((a,b,0)\)

\((a,b,d)\)

Voltage

Current

Filling with \(\varepsilon\) and \(\mu\)

\[
Z_{ij}^{pp}(\omega) \approx \frac{j \omega \mu d}{ab} \cdot \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \left[ \frac{C_m^2 C_n^2}{k_{xm}^2 + k_{yn}^2 - k^2} \cdot \cos(k_{xm} x_i) \cdot \cos(k_{yn} y_i) \cdot \cos(k_{xm} x_j) \cdot \cos(k_{yn} y_j) \right]
\]

\[
k_{xm} = \frac{m \pi}{a}, \quad k_{yn} = \frac{n \pi}{b}, \quad k = \omega \cdot \sqrt{\mu \varepsilon}
\]

\[
C_m, C_n = 1 \quad \text{for} \quad m, n = 0 \quad \text{and} \quad \sqrt{\frac{2}{23}} \quad \text{otherwise}
\]
Planar Circuit Model II

\[ Z_{ij}^{pp}(\omega) = \frac{jd}{2\pi\rho_0} \cdot \sqrt{\frac{\mu}{\varepsilon}} \cdot \frac{H_0^{(2)}(k\rho_{ij})}{H_1^{(2)}(k\rho_0)} \]

\( \rho_0 = \) port radius, \( \rho_0 = \) port dist., \( k = \omega \cdot \sqrt{\mu\varepsilon} \)
Planar Circuit Model III

CIM

Separation d

Port i \((x_i, y_i)\)

Port j \((x_j, y_j)\)

Any Open Plane Edges

Voltage

Current

Filling with \(\varepsilon\) and \(\mu\)

\[
Z = U \cdot H
\]

\[
U_{ij} = \frac{k \pi a_j}{j} \left\{ \begin{array}{ll}
J_0(ka_i)J_1(ka_j)H_0^{(2)}(kR) & i \neq j \\
J_0(ka_i)H_1^{(2)}(ka_i) & i = j
\end{array} \right.
\]

\[
H_{ij} = \frac{k \eta d}{2} \left\{ \begin{array}{ll}
J_0(ka_i)J_0(ka_j)H_0^{(2)}(kR) & i \neq j \\
J_0(ka_i)H_0^{(2)}(ka_i) & i = j
\end{array} \right.
\]
Effect of Multiple Scatterings

Fields “seen by” CRM & RWG

Fields “seen by” CIM

Including Striplines

Trace between planes:
2 Modes: Stripline + Parallel Plate

- Stripline Mode
- Parallel Plate Mode (pp)
Complete Model for One Cavity

\[
\begin{bmatrix}
V \\
I_u
\end{bmatrix}_u + \begin{bmatrix}
0 & Y_{vu} \\
Y_{vl} & 0
\end{bmatrix} + \begin{bmatrix}
Y_{pp} & -Y_{pp} \\
-Y_{pp} & Y_{pp}
\end{bmatrix} + \begin{bmatrix}
-\mathbf{Y}_d & 0 \\
0 & (k+1)\cdot\mathbf{Y}_d
\end{bmatrix} + \begin{bmatrix}
(k^2 + k)\cdot\mathbf{Y}_d \\
-(k^2 + k)\cdot\mathbf{Y}_d
\end{bmatrix} = \begin{bmatrix}
I_u \\
I_l
\end{bmatrix} \cdot \begin{bmatrix}
V \\
V_l
\end{bmatrix}
\]

Complete Model for Full PCB

Decoupling capacitor model

Cavity representation

Cavities merged using segmentation techniques

Port 1

Port k

Port n

Comparison with Full-Wave Results

6 Vias, 4 traces case
Centered striplines at two levels, and thru vias in a 6 cavity stackup

<table>
<thead>
<tr>
<th>Port 1,3</th>
<th>Port 2,4</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 mil</td>
<td>12 mil</td>
</tr>
<tr>
<td>12 mil</td>
<td>12 mil</td>
</tr>
<tr>
<td>12 mil</td>
<td>12 mil</td>
</tr>
<tr>
<td>12 mil</td>
<td>12 mil</td>
</tr>
</tbody>
</table>

Centered striplines at two levels, and thru vias in a 6 cavity stackup

<table>
<thead>
<tr>
<th>Model</th>
<th>FEM simulation</th>
<th>FIT simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency [GHz]</td>
<td>Magnitude of S\textsubscript{12 (dB)}</td>
<td>Magnitude of S\textsubscript{14 (dB)}</td>
</tr>
</tbody>
</table>

Graph showing comparison of Model, FEM simulation, and FIT simulation results for S\textsubscript{14} Magnitude.
## Comparison with Full-Wave Results

### Computation Times Obtained by Different Methods

<table>
<thead>
<tr>
<th>Method</th>
<th>Time</th>
<th>Network Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Finite element method simulation (200 freqs)</td>
<td>11 144 s (~3 h 5 min)</td>
<td>Computed on a 3.0 GHz PC, with 4GB RAM.</td>
</tr>
<tr>
<td>Finite integration technique simulation</td>
<td>24 804 s (~4 h 53 min)</td>
<td></td>
</tr>
<tr>
<td>Proposed models (200 frequency points)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cavity model double sum, 100x100 modes</td>
<td>23 s</td>
<td></td>
</tr>
<tr>
<td>Cavity model single sum, 50 iterations</td>
<td>9 s</td>
<td></td>
</tr>
</tbody>
</table>

Field information available

High level description (text-based)

3D Model required

Network Parameters

**Computation is 2 to 3 orders of magnitude faster in comparison to general-purpose numerical methods!**

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Comparison with Measurements

Assumption of infinite plates

- 119 vias (76 signal, 43 ground)
- 14 differential striplines (2D)
- 6 cavities
- Terminations

Comp. time: < 3 min

Comparison with Measurements

Models capture the salient features of the hardware response despite simplifications.
Comparison with Measurements

Simulation of the time domain link performance up to 15 Gbps within 10% accuracy!
Physics based via models can predict SI, PI, and EMC issues on PCBs up to tens of GHz

- They do this (very) efficiently
- They do this (quite) accurately
- ... but limitations exist with regard to shape, size, and proximity of vias!
(4) Application Example
1. Design of Controlled Vias

Calculation of Ground and Displacement Return Currents using CIM

\[
\begin{align*}
&\text{Port } i \quad \text{Port } j \\
&\varepsilon_r \\
&d \\
&d_g \\
&2 \cdot r_{\text{sigvia}} \\
&2 \cdot r_{\text{gndvia}}
\end{align*}
\]
1. Design of Controlled Vias

Effect of Number of Ground Vias

![Diagram showing the effect of number of ground vias on normalized displacement current.](image)
1. Design of Controlled Vias

Engineering Rules for Design

1.) The number of ground vias should always be $\geq 2$!

2.) The aperture $s$ should not exceed $0.08 \cdot \lambda$ where $\lambda$ is the wavelength at $20$ GHz for a normalized displacement current of less than $10\%$!

$s = 2 \cdot \left( d_g \sin \frac{\alpha}{2} - r_{\text{gndvia}} \right) \quad \alpha = 360^\circ/N_{\text{gnd}}$
1. Design of Controlled Vias

Application Example

The via shows a typical transmission line behavior (reflection)

The transmission is above -1dB up to 40GHz

13 layers
Application Examples – Summary

- Physics based via models can be used to mitigate common SI and PI issues
- They are especially useful for pre-layout analysis
- Due to their efficiency PCB layout automation and optimization become „viable“
Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards

S. Müller, Student Member, IEEE, F. Happ, X. Duan, Member, IEEE, R. Rimolo-Donadio, Member, IEEE, H.-D. Brüns, and C. Schuster, Senior Member, IEEE

Abstract—This paper presents for the first time the comprehensive modeling of complete via constellations of up to 10,000 elements in multilayer printed circuit boards with up to 8 cavities using the physics-based approach. For each computational step of the physics-based approach, several alternatives are analyzed with regard to their computational efficiency, and calculation times are discussed as a function of the number of simulated vias. The results of this analysis are used in combination with previous studies to determine an efficient yet accurate algorithm for the simulation of large numbers of vias. The impact of the stackup configuration on the computational effort of the algorithm is analyzed, and the most computationally expensive parts of the calculation process are identified. A parallelization of the algorithms is carried out to accelerate the critical calculation tasks. As an evaluation example, simulation results for a via array consisting of 10,000 vias and 8 cavities are shown. With the proposed simulation methods, the computation time for this via array is about 6.5 hours per frequency point on a single CPU and about 40 minutes per frequency point with the parallel version running on 16 CPUs.

Index Terms—through-hole via, multilayer printed circuit board, equivalent circuit model, computational electromagnetics

1. INTRODUCTION

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