IBIS + Mpiolog: Current and Future Developments on I/O-Buffer Modeling

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Agenda

1. Macromodels for SI&PI: Requirements
2. IBIS, Two-piece Macromodels & Power-Awareness (?)
3. Enhanced Macromodels (Mpiolog-class)
4. Possible Enhancements to IBIS
5. Conclusions
Requirements for I/O Macromodels

Accuracy at Output Port \((v(t), i(t))\)
+ Supply-Current Profile \((i_{dd}(t))\)
+ Supply-Voltage Noise \((v_{dd}(t))\)
+ Supply-Noise Effects \((f(\Delta v_{dd}))\)

= I/O-buffer model for SI&PI

Targets:
\[
\begin{align*}
    v(t), i(t) \\
    v_{dd}(t), i_{dd}(t) \\
    \Delta t, \Delta v_{out}, \Delta i_{dd} = f(\Delta v_{dd})
\end{align*}
\]
Two-piece Model Structure

Example: Single-Ended Output Buffer

Pre-Driver
Zout \rightarrow e.g., UP/DN = <11001>
Slew-Rate (SR) control:
changing UP/DN<n:1> over time

Output Stage
(n-replica)

Power Clamp

Ground Clamp

Pre

Driver

\text{Power}

\text{Clamp}

\text{Ground}

\text{Clamp}

\text{Physical}

\text{Topology}

\text{*DUM} = \text{Device Under Modeling}
Two-piece Model Structure

Example: Single-Ended Output Buffer

Pre-Driver
Zout → e.g., UP/DN=<11001>
Slew-Rate (SR) control:
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(n-replica)

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Physical Topology

Two-piece Model

\[ i(t) = w_H(t) \cdot I_{PU}(v) + w_L(t) \cdot I_{PD}(v) - C_{COMP} \frac{\partial v}{\partial t} \]

Up/Down Events

Pull-Up

Pull-Down

“Dynamic”
IBIS v3.2 & Two-piece Model Structure

my_ibis.ibs

[Model]
[Pull-Up]
\[ v_1 \quad i_1 \]
\[ v_2 \quad i_2 \]
...
[Pull-Down]
[C_comp]
[Rising Waveform]
\[ t_1 \quad v_1 \]
\[ t_2 \quad v_2 \]
...
[Falling Waveform]

\[ i(t) = w_H(t) \cdot I_{PS}(v(t)) + w_L(t) \cdot I_{PD}(v(t)) - C_{COMP} \frac{\partial v}{\partial t} \]

IBIS v3.2 Equivalent Electrical Circuit

\[ i(t), v(t) @ VDD_{NOM} = \smiley \]

⚠️ Limitation:
\[ \begin{align*}
  i_{dd}(t) &= ? / \frown
  v_{dd}(t) \neq VDD_{NOM} \Rightarrow ??? / \frown
\end{align*} \]
Power-awareness in IBIS (v5.0)

\[ i(t) = w_H(t) \cdot I_{PU}(v) + w_L(t) \cdot I_{PD}(v) - C_{COMP} \frac{\partial v}{\partial t} \]

"Power-Aware" Two-piece Model

\[ i(t) = w_H(t) \cdot K_{SSOPU} (\Delta v_{dd}) \cdot I_{PU}(v) + w_L(t) \cdot K_{SSOPD} (\Delta v_{ss}) \cdot I_{PD}(v) - C_{COMP} \frac{\partial v}{\partial t} \]

IBIS v5.0

KSSO_PU/PD introduce approximations of supply/ground noise on output static characteristics

Supply-current is explicitly modeled, and corresponds to pull-up and "crow-bar"/other current contributions
Power-awareness in IBIS (v5.0)

“Power-Aware” Two-piece Model = IBIS v5.0

\[ i(t) = w_H(t) \cdot K_{SSOPU}(\Delta v_{dd}) \cdot I_{PU}(v) + w_L(t) \cdot K_{SSOPD}(\Delta v_{ss}) \cdot I_{PD}(v) - C_{COMP} \frac{\partial v}{\partial t} \]

\[ i_{dd}(t) = w_H(t) \cdot K_{SSOPU}(\Delta v_{dd}) \cdot I_{PU}(v) + \partial i(t) \]

my_ibis_v5.ibs

IBIS v5.0 Equivalent Electrical Circuit

\[ w_H(t) \cdot K_{SSOPU}(\Delta VDD(t)) \cdot I_{PU}(v(t)) \]

\[ w_L(t) \cdot K_{SSOPD}(\Delta VSS(t)) \cdot I_{PD}(v(t)) \]
Validation

Reference (XTOR-level)

vs IBIS v5.0 😁

Supply-Noise

Supply-Current

CLK/DATA Far-End Signals
**VDD ↔ Static Characteristics**

Nested .DC sweep on Output and Supply ports

Possible inaccuracy with ISSO_PU(PD) approximation?
$V_{dd} \in [80\%, ..., 100\%, ..., 120\%] \times V_{DD,NOM}$

Switching Profiles ($w_H$, $w_L$) can have a very complex dependency with VDD variations.

IBIS v5.0 model structure may be limited in representing this behavior.
VDD ↔ Supply-Current \([I_{COMP}]\)

\[ V_{dd} \in [80\%, \ldots, 100\%, \ldots, 120\%] \times V_{DD,NOM} \]

Pre-Driver/Crowbar Current has also a complex dependency with VDD variations (timing, peak)

IBIS v5.0 model structure may also be limited in representing this behavior
How to correctly model I/O-Buffer “supply-port impedance”?

Dynamic Contribution to Supply-Current

\[ Z_{DUM}(f) \neq Z_{IBIS} = ? \]
Enhanced I/O-Buffer Macromodels

Mpiolog-class
Enhanced Two-Piece Models: R&D work

\[ i(t) = w_H(t, v_{dd}) \cdot [I_{PU}(v, v_{dd}) + f_H(v, v_{dd})] + w_L(t, v_{dd}) \cdot [I_{PD}(v, v_{dd}) + f_L(v, v_{dd})] \]

\[ i_{dd}(t) = w_H(t, v_{dd}) \cdot [I_{PU,S}(v, v_{dd}) + f_{H,S}(v, v_{dd})] + w_L(t, v_{dd}) \cdot [I_{PD,S}(v, v_{dd}) + f_{L,S}(v, v_{dd})] + \partial i(t, v_{dd}) \]

Explicit dependency with VDD in model sub-components

Mathematical structure ⇒ re-cast as Verilog-A or SPICE circuit
Proposed Enhancements: Static Characteristics

The static characteristics are now extracted with nested .DC sweeps at output and supply ports.

(e.g., 1 output, 1 supply, 1 current: 3D-surface)

\[ I_S = F(V_{out}, V_{dd}) \]

Such 3D surfaces are calculated for:

\[ I_{SH}(V_{out}, V_{dd}) \]
\[ I_{SL}(V_{out}, V_{dd}) \]
\[ I_{dd,SH}(V_{out}, V_{dd}) \]
\[ I_{dd,SL}(V_{out}, V_{dd}) \]
SVD Approximation of 3D Surfaces

\[ y \approx F(V_{out}, V_{dd}) = \sum_{k=1}^{N} \sigma_k \varphi_{1,k}(V_{out}) \varphi_{2,k}(V_{dd}) \]

SVD-approximation \[ \Rightarrow \]

- SPICE Netlist (VCVS, CCCS, ...)
- Verilog-A Code

Truncation Process:
Maximum compactness meeting target accuracy

Inlet: Static Characterization Testbench
Outlet: 3D Surface

\[ \text{Y, samples @ } V_{out}, V_{dd} \text{ from SPICE and .dc sweeps} \]
Proposed Enhancements: Dynamic Characteristics

Dedicated $v_{out}(t)$ and $v_{dd}(t)$ stimuli are applied, simultaneously.

Dynamic characteristics = rational approximations using Time-Domain Vector-Fitting (TD-VF) algorithms.

$$i_{out,H} = f(v_{out}, v_{dd})$$
(e.g., pull-up dynamic MISO TDVF model)

Similar models are computed for:

$$i_{out,H}(v_{out}, v_{dd})$$
$$i_{out,L}(v_{out}, v_{dd})$$
$$i_{dd,H}(v_{out}, v_{dd})$$
$$i_{dd,L}(v_{out}, v_{dd})$$

and implemented as:

- SPICE Netlist
- Verilog-A models
Proposed Enhancements: Weighting Functions

$V_{dd} \in [80\%, ..., 100\%, ..., 120\%] \times V_{DD,NOM}$

Weighting functions $w_H$ and $w_L$ are calculated for several $V_{dd}$ values.

This allows the creation of 3D-surfaces $w_H(t, v_{dd})$ and $w_L(t, v_{dd})$ reproducing the complex dependency of the switching events with VDD.
## Comparative Summary

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MPILOG Model Implementation

Mpiilog models can be synthesized as:

- **SPICE Netlists**
- **Verilog-A Modules**
- **IBIS (v5.1/6.0)** 😊
- **IBIS using [External Model]**

```plaintext
#include "constants.vams"
#include "disciplines.vams"

module mpiilog_model [v_in,v_io,vdd_io,ref_io,v_oe);

// ELECTRICAL VARIABLES
electrical v_in,v_io,vdd_io,ref_io,v_oe;

// PARAMETERS
parameter real PVDDcore=1; // logic core nominal voltage
parameter real PVDD=1.2;   // output power-supply nominal voltage
```

```plaintext
// MODEL STRUCTURE...
```
Validations

Reference (XTOR-level) vs IBIS v5.1 😊 vs MPILOG 😊

Supply-Noise

Supply-Current

CLK/DATA Far-End Signals
Possible Enhancements to IBIS models?
3-curve approx. of 3D-Surfaces in IBIS

How to include 3-curve approx. data in an IBIS file?

**IBIS v5.1:**

- **Model:** DDR_PAD
- **Variable:** typ, min, max
- **Temperature Range:** 25°C to 30°C, 125°C
- **Voltage Range:** 1.2V to 1.1V, 1.3V
- **Rising Waveform:**
  - Time:
    - 0 ps
    - 25 ps
    - ... 1.21 ns
    - 1.22 ns

**Process:**
- TT (Typical)
- SS (Slow)
- FF (Fast)

**VDD:**
- TYP
- MIN
- MAX

**Temp:**
- Typ
- Max
- Min

For all IBIS table...

**PU/PD**

Rising/Falling V-t
Rising/Falling I-t

1 [Model], 3 PVT Corners
3-curve approx. of 3D-Surfaces in IBIS

How to include 3-curve approx. data in an IBIS file?

For all IBIS table ...
- PU/PD
- Rising/Falling V-t
- Rising/Falling I-t

IBIS v5.1:
- “enhanced” IBIS

1 [Model], 3 PVT-Corners

1 [Model], 1 PT Corner (e.g., TT/25C)
Accuracy @SI&PI
(capture VDD-effects)
(Proposed) “Enhancements” to IBIS Models

- Removal of [ISSO PU] and [ISSO PD]
- 3-curve approximations
  - 3D PU/PD Characteristic
  - 3D Rising/Falling V-t Tables
  - 3D Rising/Falling [Composite Current]
- [DeCap Model]
  - C1 || (R2+C2) for “supply impedance”
(Proposed) “Enhanced” IBIS Models

This model structure can be implemented as Verilog-A code
Multi-variate Surfaces

Nested .DC sweep on Output and Supply ports

Nested .DC sweep on Output and Supply ports

.TRAN Rising Waveforms applying different VDD values

Static Characteristics

Abs. Static Characteristics

Interp. Error on $w_H(t, v_{dd})$

$w_H(t, v_{dd})$

$V_{dd}$ $V_{out}$ $V_{dd}$ $V_{out}$ $V_{dd}$ $V_{out}$ $V_{dd}$ $V_{out}$
Validation

Reference (XTOR-level)
- vs IBIS v5.1 😊
- vs MPILOG 😊
- vs e-IBIS 😊

Supply-Noise

Supply-Current
Conclusions

Enhanced two-piece model structure to accurately reproduce currents and voltages at output and supply ports:

✓ SVD + truncation-process for (multi-dimensional) Static Char.
✓ Multiple-Input TDVF for Dynamic Characteristics
✓ 3D switching characteristics $w(t, v_{dd})$

Flexible and modular approach using Mpiolog
Implementations possible in SPICE/Verilog-A

Identification of potential limitations of IBIS models power-awareness
Set of possible enhancements to IBIS
(3-curve approx. & VDD-effects, impedance at supply-port, ... )

Validation tests highlight excellent accuracy in SI/PI co-simulations
Thank you for the attention!