IBIS Chair's Report

Randy Wolff

Micron Technology

Chair, IBIS Open Forum
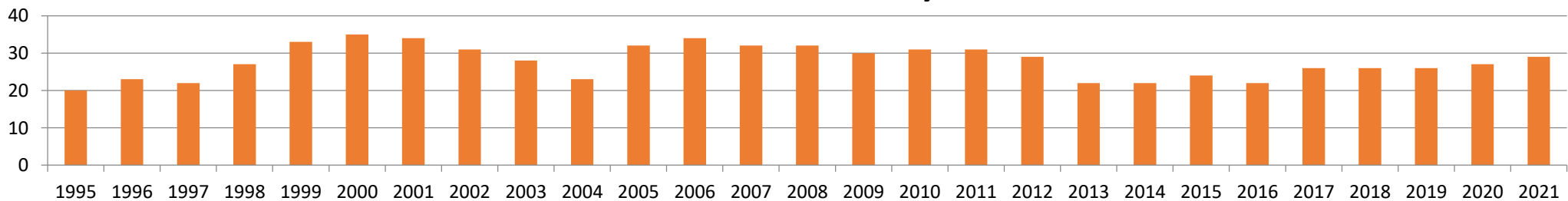
European Virtual IBIS Summit (with Virtual SPI2021)

May 12, 2021

# 29 IBIS Members (Organization-based)

Our Members

Ansys · Applied Simulation Technology · BROADCOM · cadence · Celestica

CISCO · DASSAULT SYSTEMES · Ericsson · Google · HUAWEI

IBM · Infineon · Instituto de telecomunicações · intel · KEYSIGHT TECHNOLOGIES

LUMINOUS · MARVELL · maxim integrated · Micron · MISSOURI S&T

NXP · SerDes Design.Com · SIEMENS · SiSoft · SYNOPSYS

Teraspeed Labs · XILINX · ZTE · ZUKEN

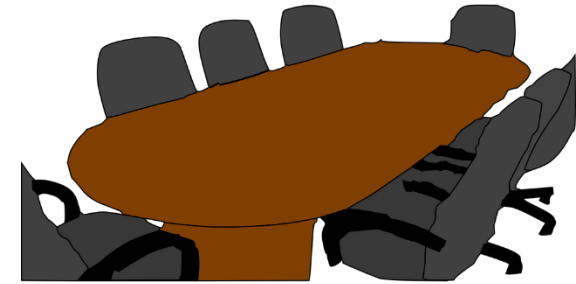**Number of Members by Year**

IBIS Officers 2020-2021

Chair: *Randy Wolff, Micron Technology*

Vice-Chair: *Lance Wang, Zuken USA*

Secretary: *Curtis Clark, ANSYS*

Treasurer: *Bob Ross, Teraspeed Labs*

Librarian: *Zhiping Yang, Waymo (Google)*

Postmaster: *Mike LaBonte, SiSoft (MathWorks)*

Webmaster: *Steve Parker, Marvell*
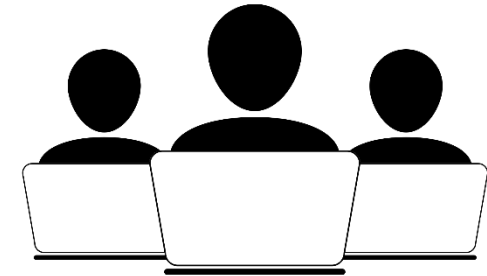
* Zhiping Yang replaced Anders Ekholm in October.

IBIS Meetings

- Weekly teleconferences
  - Quality task group (Tuesdays, 09:00 PT)
  - Advanced Technology Modeling (ATM) task group (Tuesdays, 12:00 PT)
  - Interconnect task group (Wednesdays, 08:00 PT)
    - Currently suspended as Editorial task group prepares IBIS 7.1 document
  - Editorial task group (Wednesdays, 08:00 PT)
- IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)
- IBIS Summit meetings (USA and international)
  - DesignCon, IEEE SPI, IEEE EMC+SIPI, Shanghai, Taipei, Tokyo (JEITA-organized)
- Participants: ~323 in 2020

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum

- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, and Laurie Strom

- SAE ITC provides financial, legal, and other services

- https://www.sae-itc.com/

Task Groups

- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Siemens EDA
  - https://ibis.org/atm_wip/
  - Develop non-interconnect technical BIRDs

- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/editorial_wip/
  - Produce IBIS specification documents

- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs

- Quality Task Group
  - Chair: Mike LaBonte, SiSoft (MathWorks)
  - https://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development   BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power-aware model

I/O Buffer Information Specification

- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel support
  - Interconnect modeling using IBIS-ISS and Touchstone
- 2020-2021 **IBIS 7.1 (in progress)**
  - DDRx IBIS-AMI support
  - Electrical Module Description (EMD)
  - Improved Redriver IBIS-AMI flow

Other Work

- 1995: **ANSI/EIA-656 (International standard)**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A (International standard)**
  - IBIS 3.2
- 2001: **IEC 62014-1 (International standard)**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B (International standard)**
  - IBIS 4.2
- 2009: **Touchstone 2.0**
  - Official Touchstone donated from Agilent/Keysight
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification (subset of HSPICE)
- **IBISCHK**: IBIS file syntax parser
  - Current version 7.0.2
  - Source code available for purchase
  - Compiled executables available free of charge

Planning for IBIS Version 7.1

BIRDs approved for 7.1

BIRD ID	BIRD Title	Approval Date	Notes
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models	August 31, 2018	IBIS-AMI
197.7	New AMI Reserved Parameter DC_Offset	February 21, 2020	IBIS-AMI (for DDRx)
198.3	Keyword Additions for On-Die PDN (Power Distribution Network) Modeling	August 7, 2020	Power Integrity
199	Fix Rx_Receiver_Sensitivity Inconsistencies	June 7, 2019	IBIS-AMI
200	C_comp Model Using IBIS-ISS or Touchstone	September 27, 2019	[Model] C_comp
201.1	Back-channel Statistical Optimization	July 17, 2020	IBIS-AMI
202.3	Electrical Descriptions of Modules	March 12, 2021	EMD (Next Gen EBD)
203	Submodel Clarification	April 24, 2020	Editorial
~~204~~	~~DQ_DQS GetWave Flow for Clock Forwarding Modeling~~	~~June 26, 2020~~	Superseded by BIRD209
205	New AMI Reserved Parameter for Sampling Position in AMI_Init Flow	June 26, 2020	IBIS-AMI
206	Clarification of text "transition time"	September 18, 2020	Editorial
207	New AMI Reserved Parameters Component_Name and Signal_Name	October 9, 2020	IBIS-AMI (for DDRx)
208	Clock-Data Pin Relationship Keyword	January 8, 2021	IBIS clock/data relationship
209	Make Clock Times Output Required for Clock Executable Models	March 12, 2021	IBIS-AMI (for DDRx)

Note: BIRD204 superseded by BIRD209

Planning for IBIS Version 7.1

BIRDs expected to be approved

BIRD ID	BIRD Title	Tentative Vote Date	Notes
211.x	New Redriver Flow	June 4, 2021	IBIS-AMI Redrivers
212	Clarification of PAM4_UpperThreshold, PAM4_CenterThreshold, PAM4_LowerThreshold	May 14, 2021	Editorial

Other BIRDs

BIRD ID	BIRD Title	Expected Status
166.4	Resolving problems with Redriver Init Flow	To be rejected
181.1	I-V Table Clarifications	To be delayed
190	Clarification for Redriver Flow	To be rejected
210	New Redriver AMI Flow	To be rejected (in favor of BIRD211.x)
213	Extending IBIS-AMI for PAMn Analysis	To be determined

What's Next for IBIS?

- IBIS has traditionally focused on I/O buffers and interconnect, for:
  - Solving signal integrity issues from channel loss, inter-symbol interference (ISI), and crosstalk
  - Generating waveforms or eye diagrams for timing or bit-error-rate analysis
- IBIS must continue to evolve to meet both the SI and PI demands of new signaling technologies
  - System-level perspective
    - Clock/data relationships, timing information, equalization training
  - Power Distribution Network (PDN) is a critical piece of overall system design
  - Potential for IBIS to enable improved modeling/analysis of PDN
    - Voltage regulator models
    - Chip power models

Submitting Your Idea – BIRD Process

- BIRD – Buffer Issue Resolution Document
  - Official method for submitting a proposed change to the IBIS specification
- BIRD template found on IBIS website
  - Standardizes method to describe your idea
- Submit BIRD to chair@ibis.org
- BIRDs discussed in Open Forum meetings
  - Eventual vote by members for approval
- Idea not ready for an official BIRD?
  - Join an IBIS Task Group meeting for technical discussion

BIRD Link on IBIS Website

Link to BIRDs webpage

BIRD Template Link on the BIRD Webpage

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
213	Extending IBIS-AMI for PAMn Analysis	Walter Katz, The MathWorks, Inc	May 5, 2021		
212	Clarification of PAM4_UpperThreshold, PAM4_CenterThreshold, PAM4_LowerThreshold	Hansel Desmond Dsilva, Achronix Semiconductor	April 13, 2021		
211.1	New Redriver Flow	Walter Katz, The MathWorks, Inc	March 23, 2021, April 21, 2021		
210	New Redriver AMI Flow	Fangyi Rao, Keysight Technologies	February 19, 2021		
209	Make Clock Times Output Required for Clock Executable Models	Arpad Muranyi, Siemens Digital Industries Software	January 28, 2021	March 12, 2021	
208	Clock-Data Pin Relationship Keyword	Michael Mirmak, Intel Corp.	October 6, 2020	January 8, 2021	
207	New AMI Reserved Parameters Component_Name and Signal_Name	Randy Wolff, Micron Technology	July 29, 2020	October 9, 2020	
206	Clarification of text "transition time"	Hansel Desmond Dsilva, Achronix Semiconductor; Walter Katz, Signal Integrity Software; Fangyi Rao, Keysight; Todd Bermensolo, Keysight; Arpad Muranyi, Mentor Graphics.	June 26, 2020	September 18, 2020	
205	New AMI Reserved Parameter for Sampling Position in AMI_Init Flow	Hansel Desmond Dsilva, Achronix Semiconductor; Walter Katz, Signal Integrity Software; Todd Bermensolo, Keysight; Fangyi Rao, Keysight; Arpad Muranyi; Mentor Graphics; Ambrish Varma, Cadence	May 14, 2020	June 26, 2020	
204	DQ_DQS GetWave Flow for Clock Forwarding Modeling	Walter Katz, The MathWorks Fangyi Rao, Keysight Wendem Beyene, Intel Ambrish Varma, Cadence	April 22, 2020	June 26, 2020	
203	Submodel Clarification	Randy Wolff, Micron Technology	March 10, 2020	April 24, 2020	
202.3	Electrical Descriptions of Modules	Walter Katz, Signal Integrity Software; Justin Butterfield, Micron Technology; Curtis Clark, ANSYS; Arpad Muranyi, Siemens Digital Industries Software; Michael Mirmak, Intel Corp.; Bob Ross, Teraspeed Labs; Lance Wang, Zuken USA; Randy Wolff, Micron Technology	January 22, 2020, October 29, 2020; January 27, 2021; February 19, 2021	March 12, 2021	

[Thank You]

IBIS Open Forum:
Web: https://www.ibis.org
Email: info@ibis.org

We welcome participation
by all IBIS model makers,
EDA tool vendors, IBIS model
users, and interested parties.