IBIS power current prediction at overclocked datarates

SPI Virtual IBIS Summit
May 26, 2022

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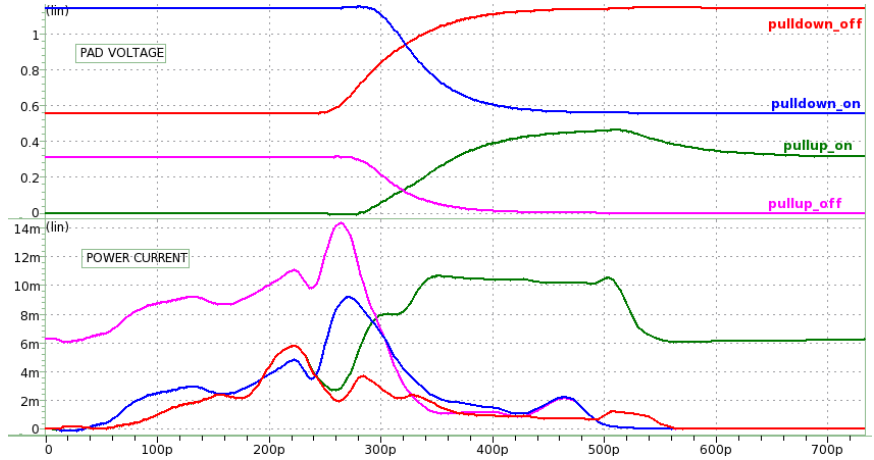
What is IBIS overclocking?

Example of voltage and current waveforms of an IBIS buffer model



- IBIS model characterizes/describes the dynamic behavior of an output or I/O buffer, by mean Rise/Fall V/t tables (voltage versus time)
  - In power aware IBIS models the corresponding power current profiles are also provided (Composite Current tables)
  - Transient waveforms extracted with 2 load conditions (usually: 50 ohm to ground, 50 ohm to power)
  - EDA tool will use the data for building an internal model of the driver and predict the circuit behavior for any generic load condition
  - EDA tool driver model (based on the IBIS data): made of current sources controlled by specific equations. This is often referred to as the 2 equations, 2 unknowns algorithm.
- Time duration of these transient voltage and current waveforms should be long enough in order to have them settled (with a final steady state value reached)
- When simulation UI is shorter than IBIS transient waveform duration, then the resulting voltage and current waveforms do not have the needed time to settle
  - A new switching transition happens before that the previous one is completed
  - This condition is known as overclocking
- Overclocking can determine a loss of accuracy of the IBIS simulation (compared to the corresponding golden reference transistor level simulation)
  - Due to the IBIS algorithm (implemented in the EDA simulation tool) not able to replicate/predict the ‘overclocked’ voltage and current profiles

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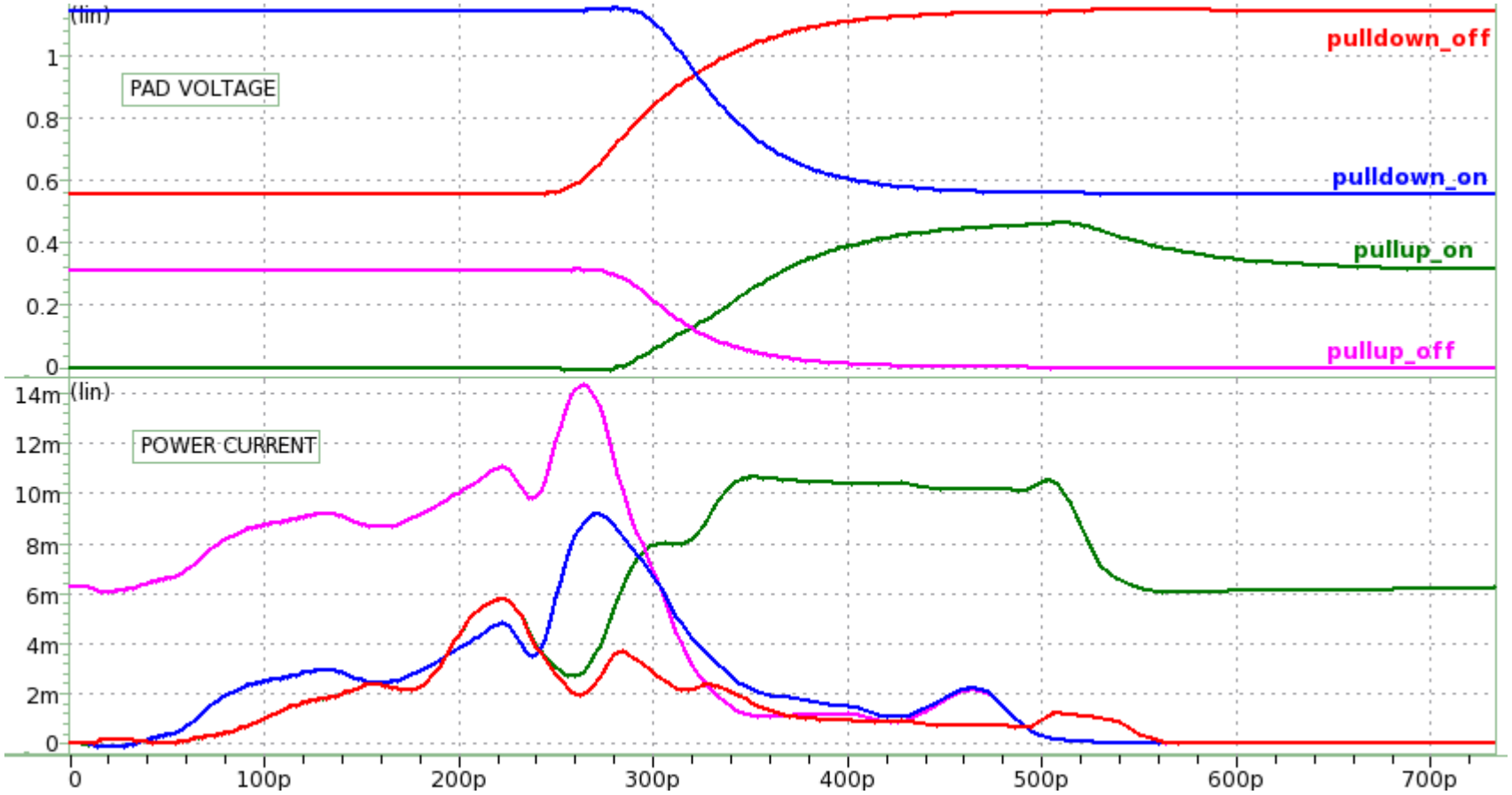
Overclocking test simulation

- Output buffer IBIS model (related to the ONFI interface of a micro-controller)
- IBIS results compared to the corresponding transistor level (TL) sim
- Minimum corner
- IBIS V/t & I/t curves duration: UI_{IBIS}=732ps
- Overclocked sim at 3600 Mbps → UI_{SIM}=277ps < UI_{IBIS}=732ps
- Simple load: 50 ohm to ground, with pulse input stimulus
  - Same load as used for generating 2 of the 4 IBIS transient curves
  - At lower datarates: IBIS sim results (voltage and current waveforms) perfectly match the corresponding TL sim
  - At over-clocked datarates: IBIS results are not accurate as expected
- The driver also has a fixed-time pre-emphasis
  - immediately after a switching transition the Ron is boosted to a lower Ron value, for a limited and fixed amount of time

IBIS V/t and I/t curves: minimum UI constraint



- IBIS transient curve duration (min corner)=732ps
- IBIS minimal transient curve duration, after removing initial delays of V/t curves, handled by simulator overclocking algorithm:
  496ps
- IBIS over-clocking limit: 496ps
- Target datarate 3600Mbps
  UI=277ps
  overclocking limit is exceeded

pullup_on	rise 50 ohm to gnd
pullup_off	fall 50 ohm to gnd
pulldown_on	fall 50 ohm to pwr
pulldown_off	rise 50 ohm to pwr

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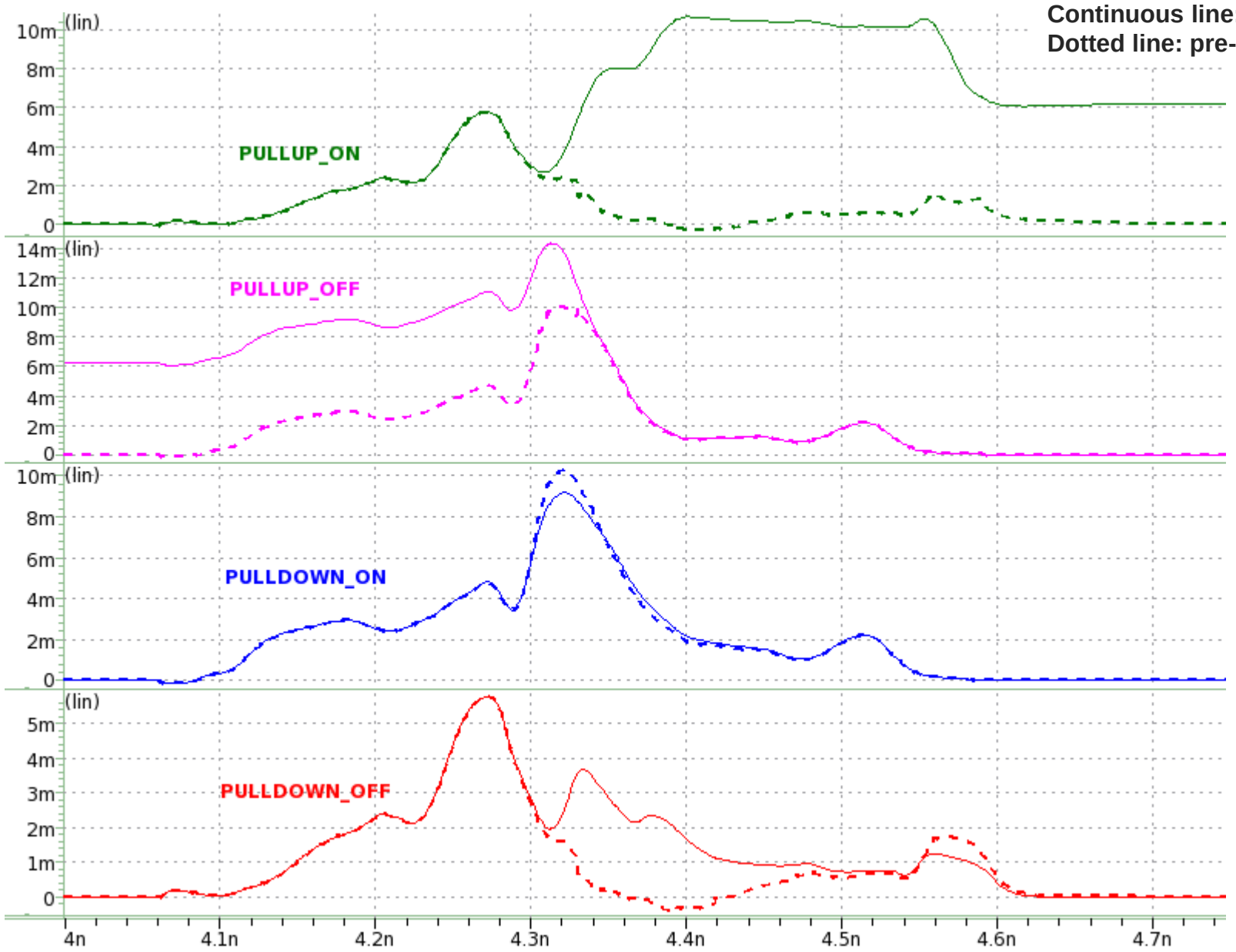
IBIS I/t curves: pre-driver current



- For having an accurate power noise modelling it is important to capture all the current on the VCCQ rail
- In this IO design the pre-driver stage shares the same VCCQ power domain as the final driver
- Pre-driver current is included in the IBIS composite current curves

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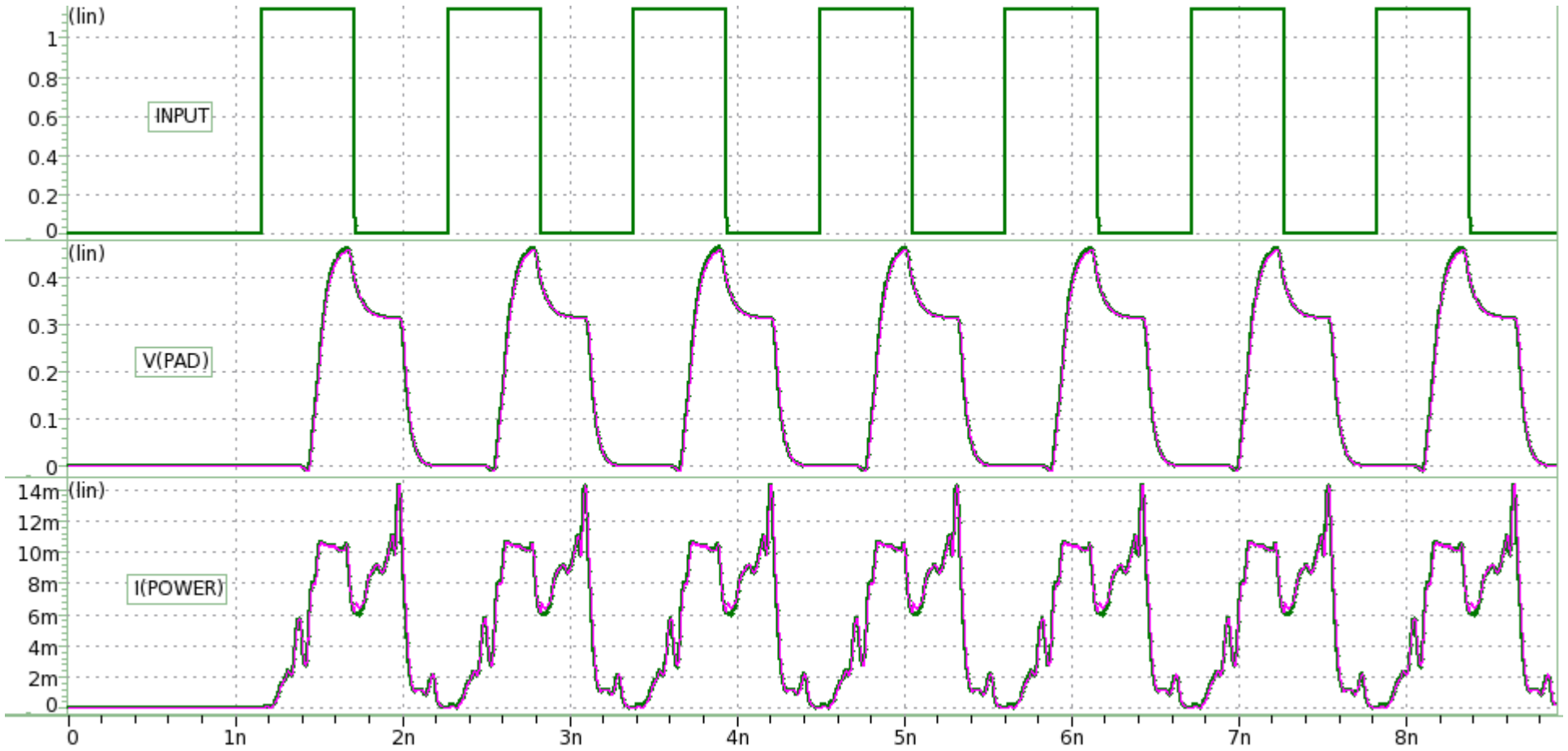
IBIS vs TL @1800 Mbps (no overclocking)

Transistor Level (TL)
IBIS



- UI_{sim}=555ps > $UI_{IBIS\text{-}reduced}$=496ps (no over-clocking)
- IBIS power current matches TL results

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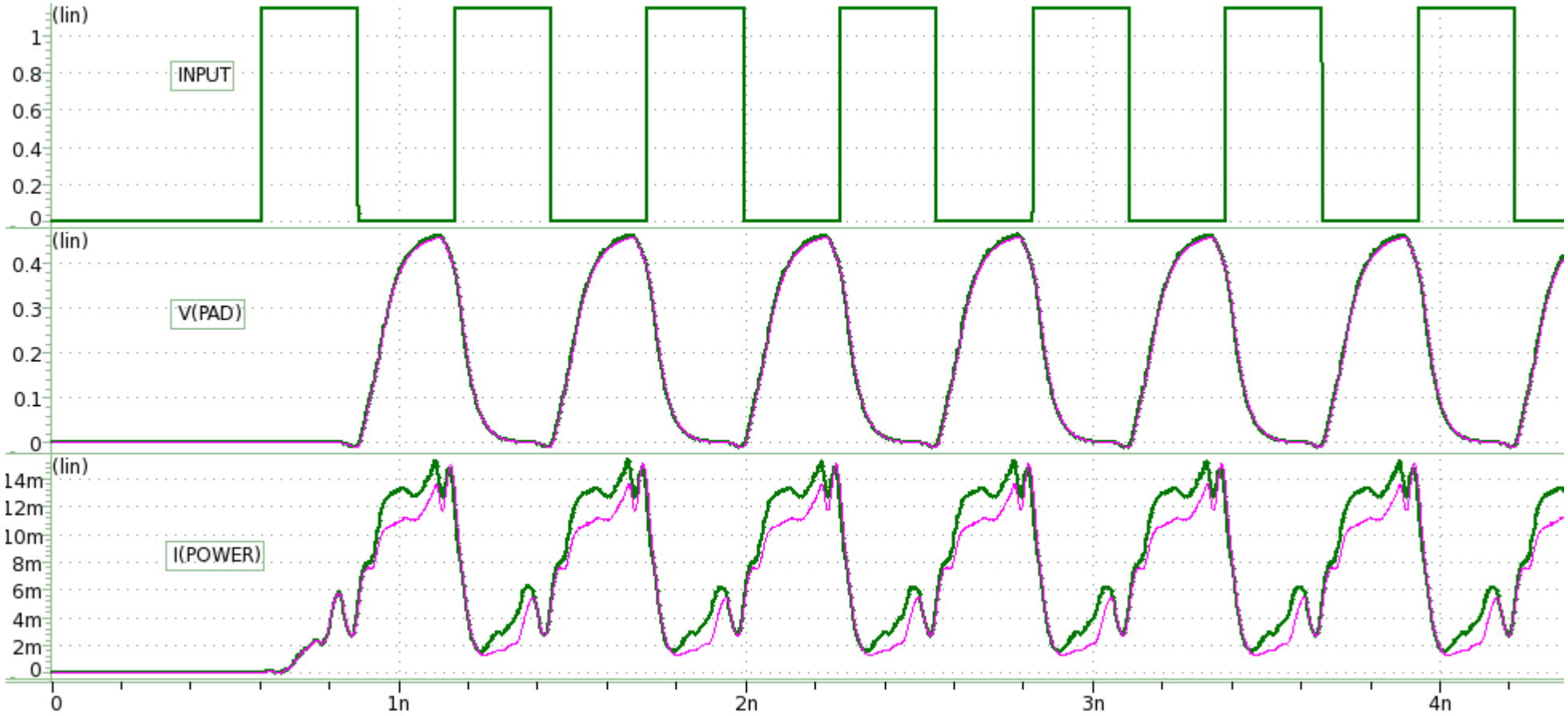
IBIS vs TL @3600 Mbps (overclocking)

Transistor Level (TL)
IBIS



- UI_{sim}=277ps < $UI_{IBIS\text{-}reduced}$=496ps (over-clocking)
- IBIS power current does not match TL results
- Can the IBIS over-clocking algorithm be improved in EDA tools in order to predict a more accurate power current profile?

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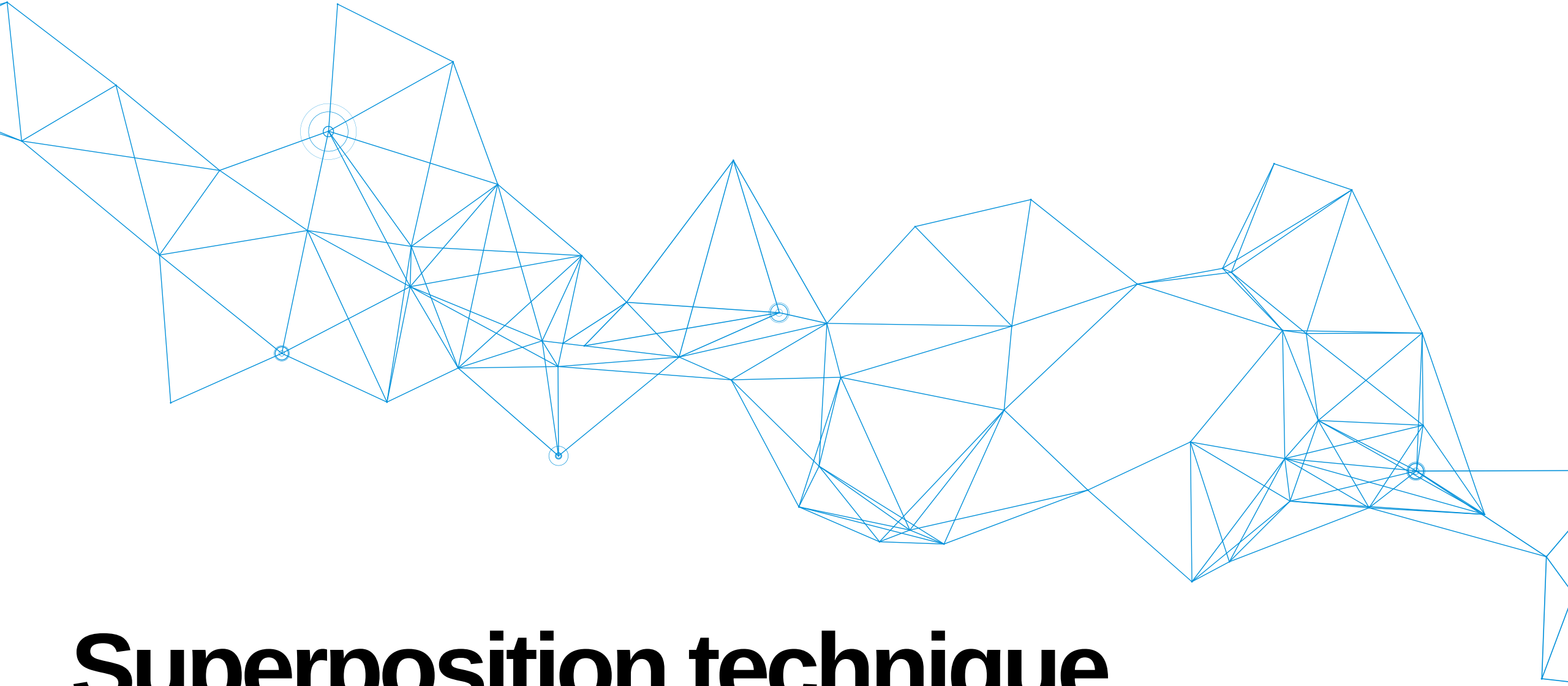

Superposition technique

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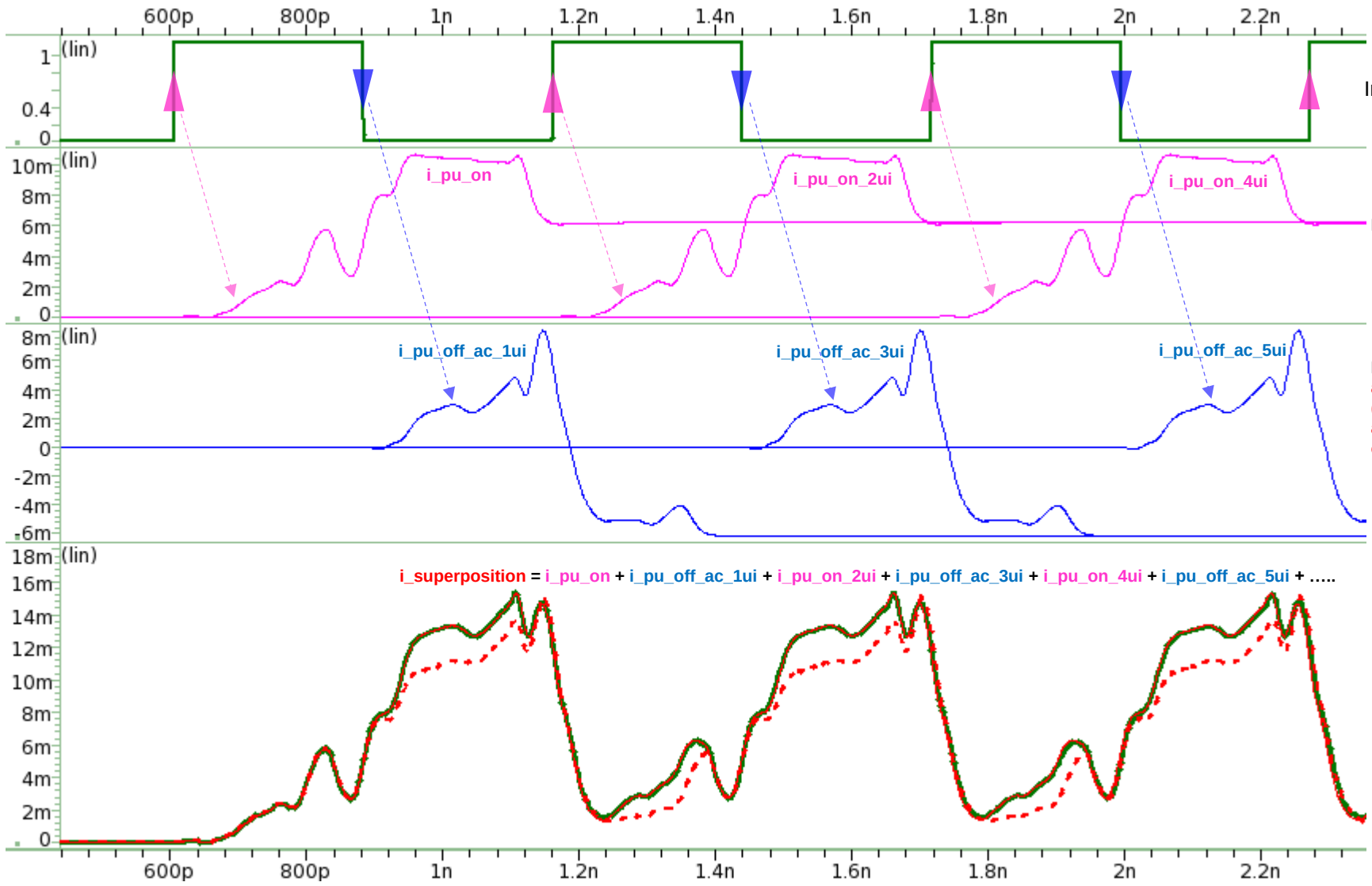
Composite currents superposition technique 1/2

- Power current waveform: can be obtained by applying a superposition of the IBIS composite currents waveforms
  - IBIS composite current waveforms summed together after a proper time translation, for having them synchronous with the input stimulus
  - DC value double counting to be avoided – DC value is already considered in the first composite current waveform, must be subtracted from the other ones
- Tested initially for a simple test-load: 50 ohm to ground
  - Same load as used for 2 of the 4 V/t (and composite current) curves in the IBIS model (pullup-on, pullup-off)
  - Pullup-on waveform triggered from rising-edge of the input stimulus
  - Pullup-off triggered from falling edge
- Superposition applied by using a waveform viewer tool
  - Custom equations can be defined for combining together multiple voltage/current waveforms
  - The needed post-processing operation are available: algebraic sum, time translation

Composite currents superposition technique 2/2



Input stimulus

IBIS pullup-on composite currents

IBIS pullup-off composite currents, after subtracting the initial DC value (to avoid double counting, because already included in the pullup-on composite currents above)

IBIS composite currents, time translated (synchronized with the input trigger events)

Power current:

- green: from TL
- dotted red: EDA tool IBIS sim result
- continuous red: superposition result

IBIS overclocking algorithm is suitable for improvements

- Based on the performed tests it seems that the IBIS algorithm of the commercial simulators is not very good in predicting the power current profile (there is room for improving it)
- A possible improvement has been suggested and tested: IBIS composite currents superposition technique
  - Composite current curves to be summed after a proper time translation (for syncing them with the input trigger events)
- The IBIS model already contains the needed data for a more accurate power current prediction also at overclocked datarates
  - Demonstrated for a basic test-load (50 ohm to ground)
  - To be tested also for more generic test-loads
- The suggested technique was also proposed by Synopsys (more than 10 years ago)
  - Described in the IBIS Summit presentation “An Effective Solution to Simulate Composite Current When Over-clocking” by Xuefeng Chen (2014, November 14)
  - https://www.ibis.org/summits/nov14a/chen.pdf
  - But not widely adopted until now
- Collaboration between Micron and Synopsys for testing the superposition technique
  - Tested by Micron with different test-loads and IBIS models

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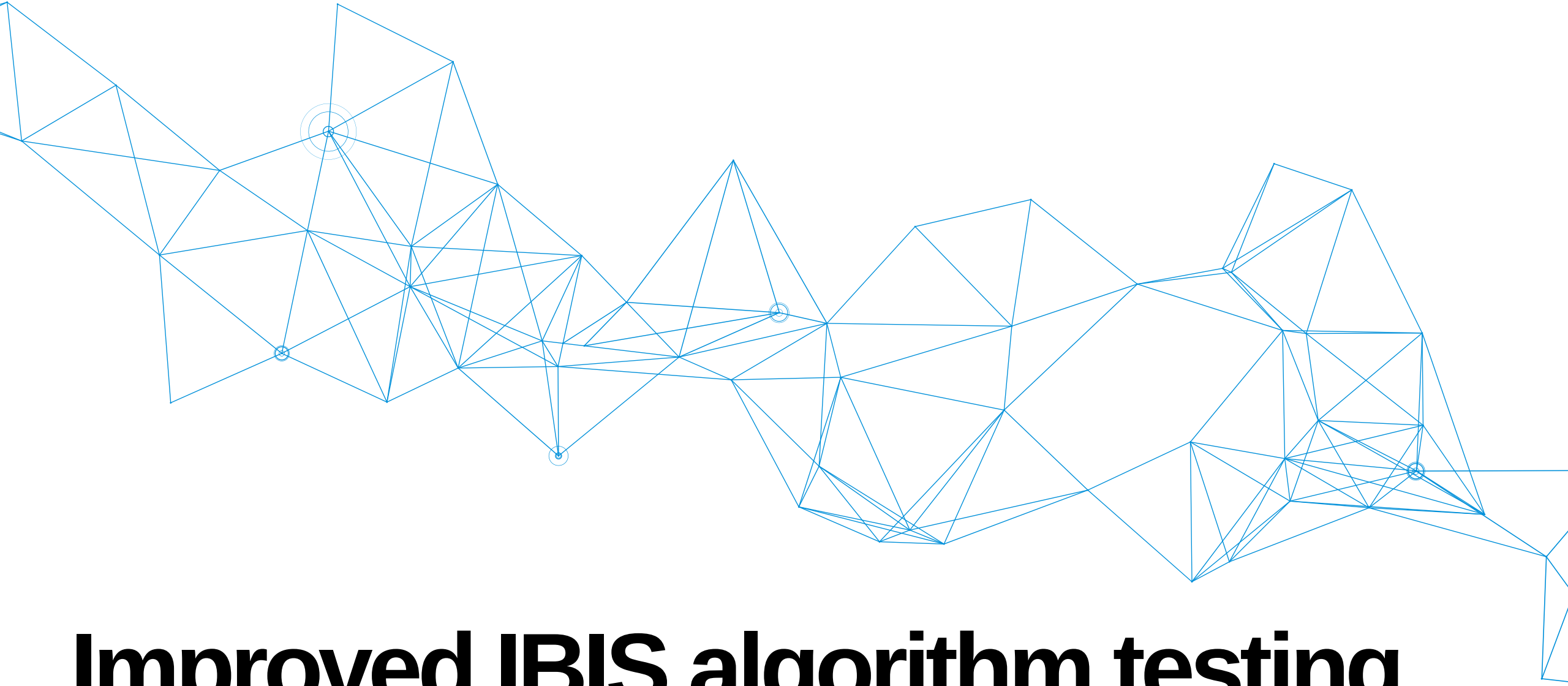

Improved IBIS algorithm testing

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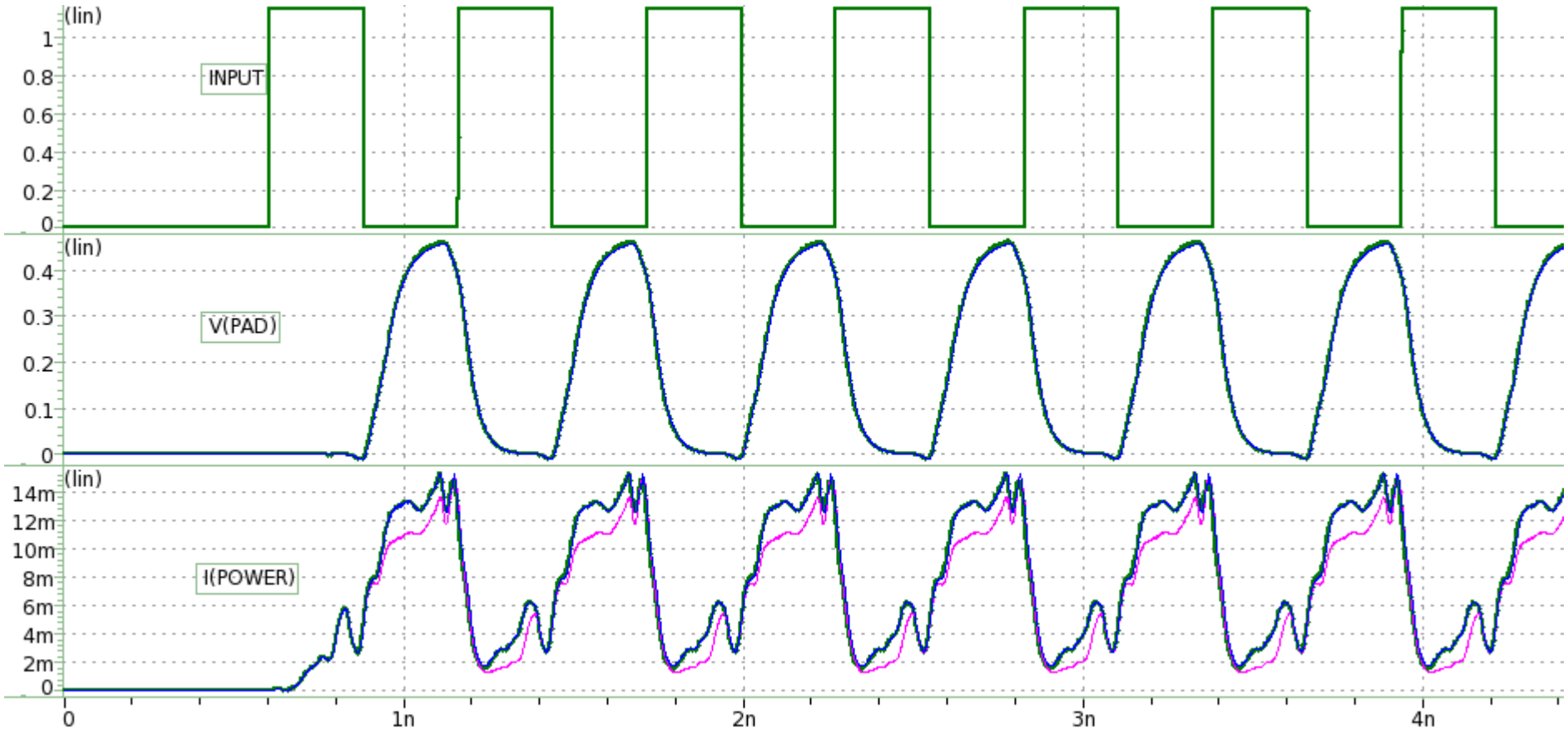
Test with 50 ohm to gnd load

UI_{sim}=277ps < $UI_{IBIS\text{-}reduced}$=496ps (over-clocking)



Transistor Level (TL)
IBIS EDA tool old
IBIS EDA tool new

- Simple 50-ohm to ground test-load
- IBIS power current (with the new enhanced IBIS algorithm) now matches TL results

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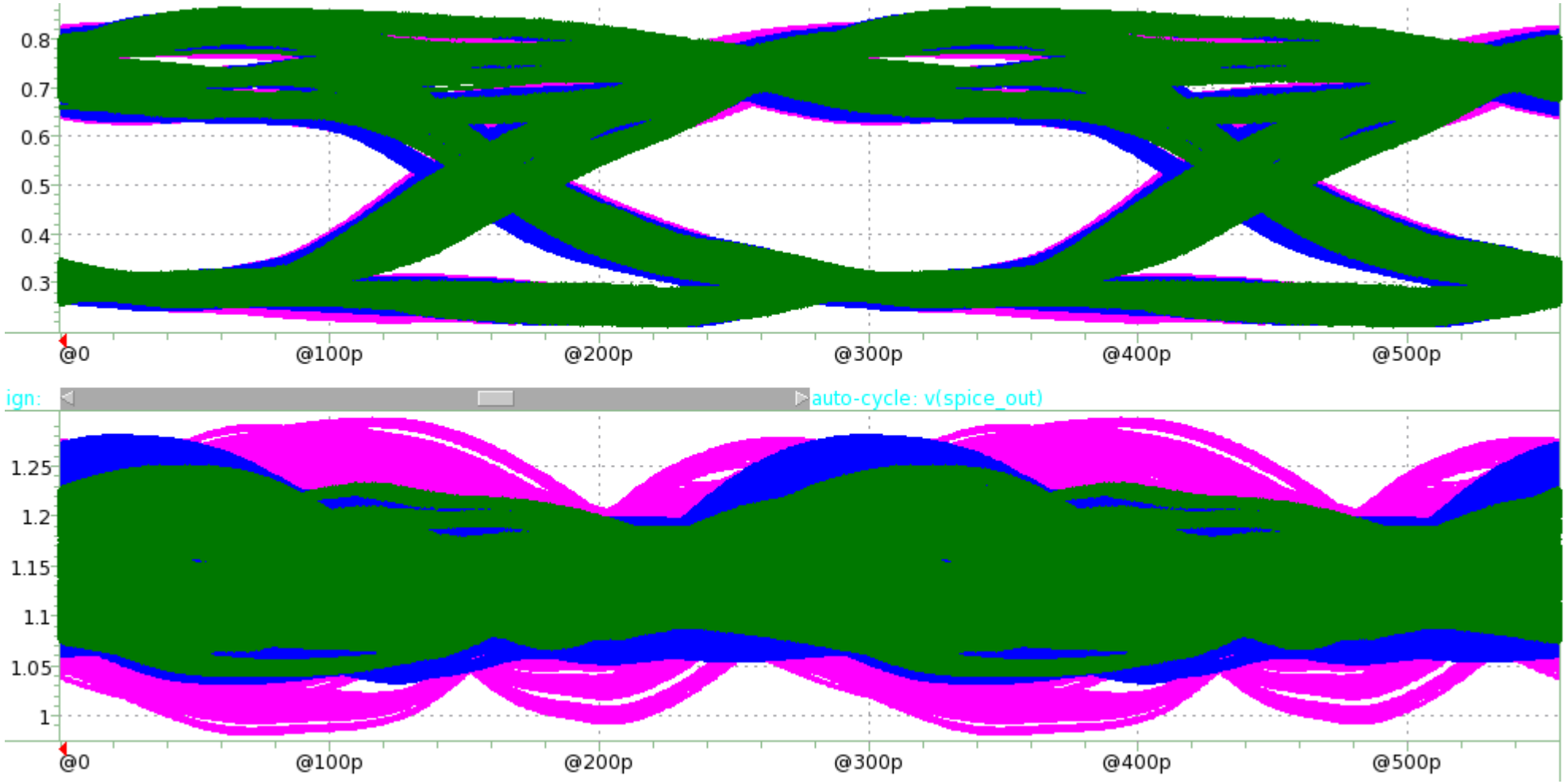
Test with real load and noisy power 1/3

Transistor Level (TL)
IBIS old
IBIS new



Output voltage eye diagram

Power voltage (in sync with eye diagram)

- Load: 150ps T-line, 2pF, 50 ohm to VCCQ/2
- Pkg parasitics for power, ground and data signal; with reduced on-die decoupling (in order to have a noisy power voltage)
- Input pattern: PRBS, nr of bits: 2^14

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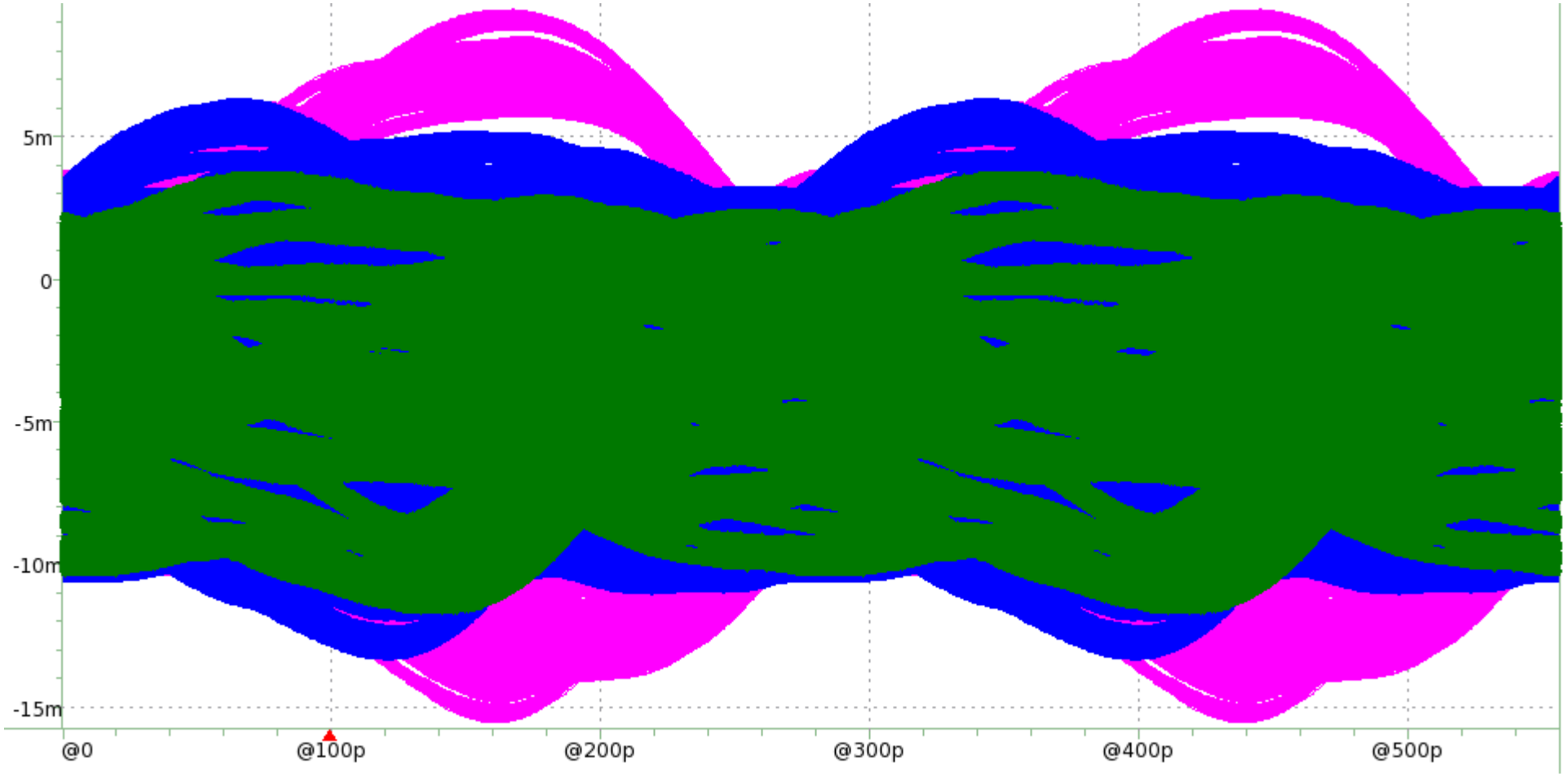
Test with real load and noisy power 2/3

Transistor Level (TL)
IBIS old
IBIS new



Power current
(in sync with eye diagram)

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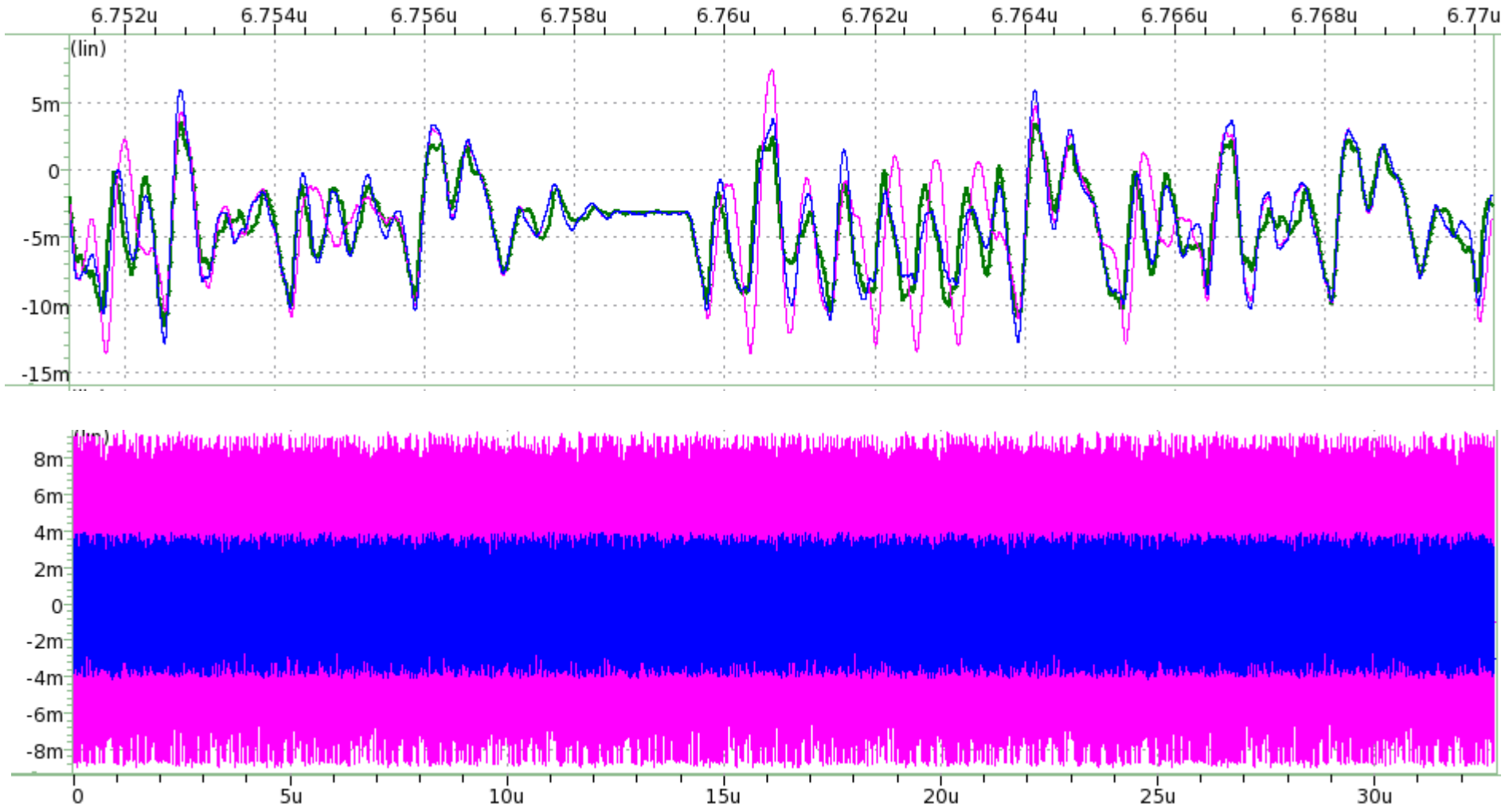
Test with real load and noisy power 3/3

Transistor Level (TL)
IBIS old
IBIS new



Power current zoomed-in

Power current error (TL – IBIS)

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Test with another IBIS model

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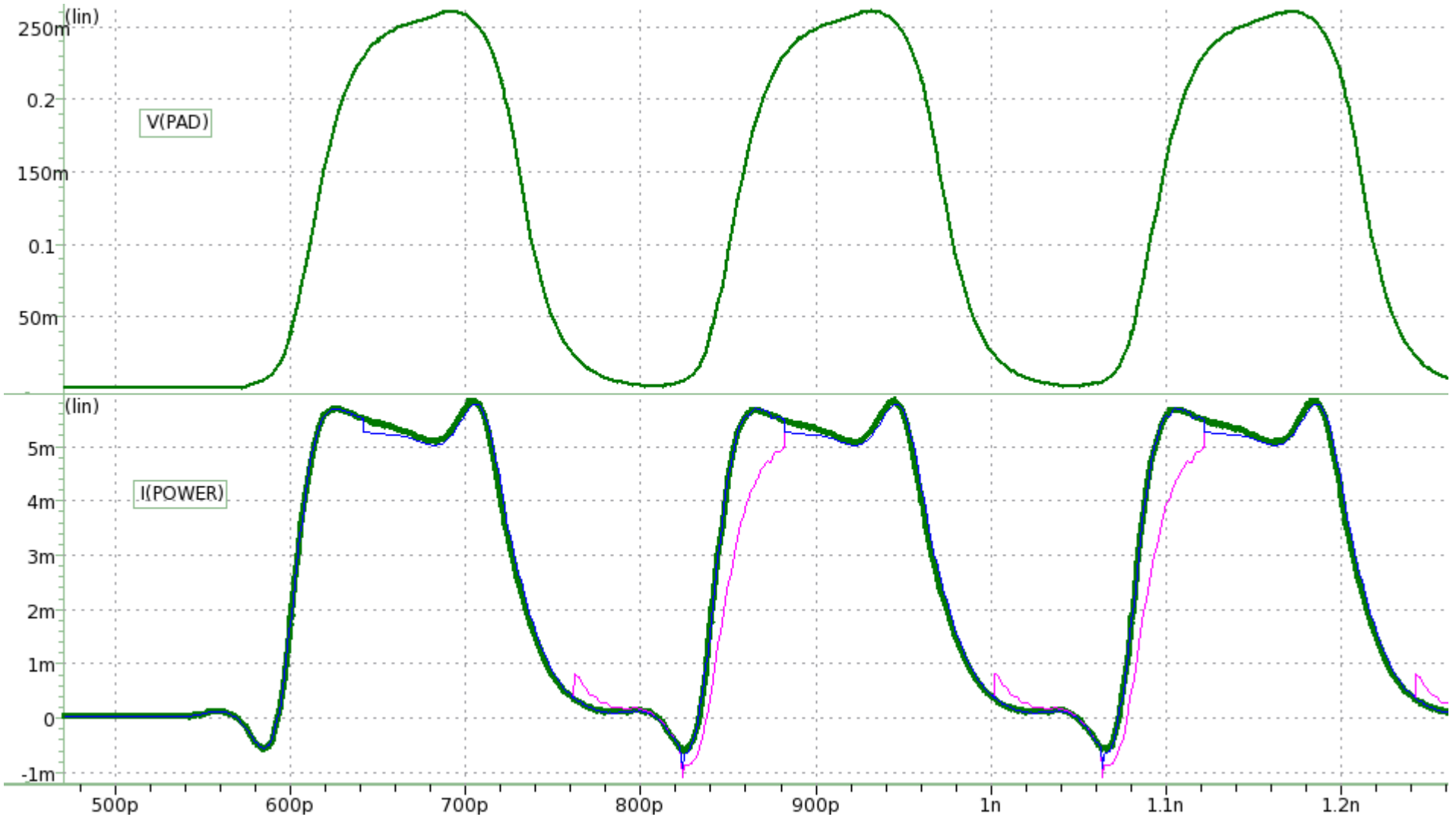
DDR5 IBIS - with 50 ohm load



Transistor Level (TL)
IBIS old
IBIS new

IBIS UI = 319p
SIM UI = 120p (8333 Mbps)

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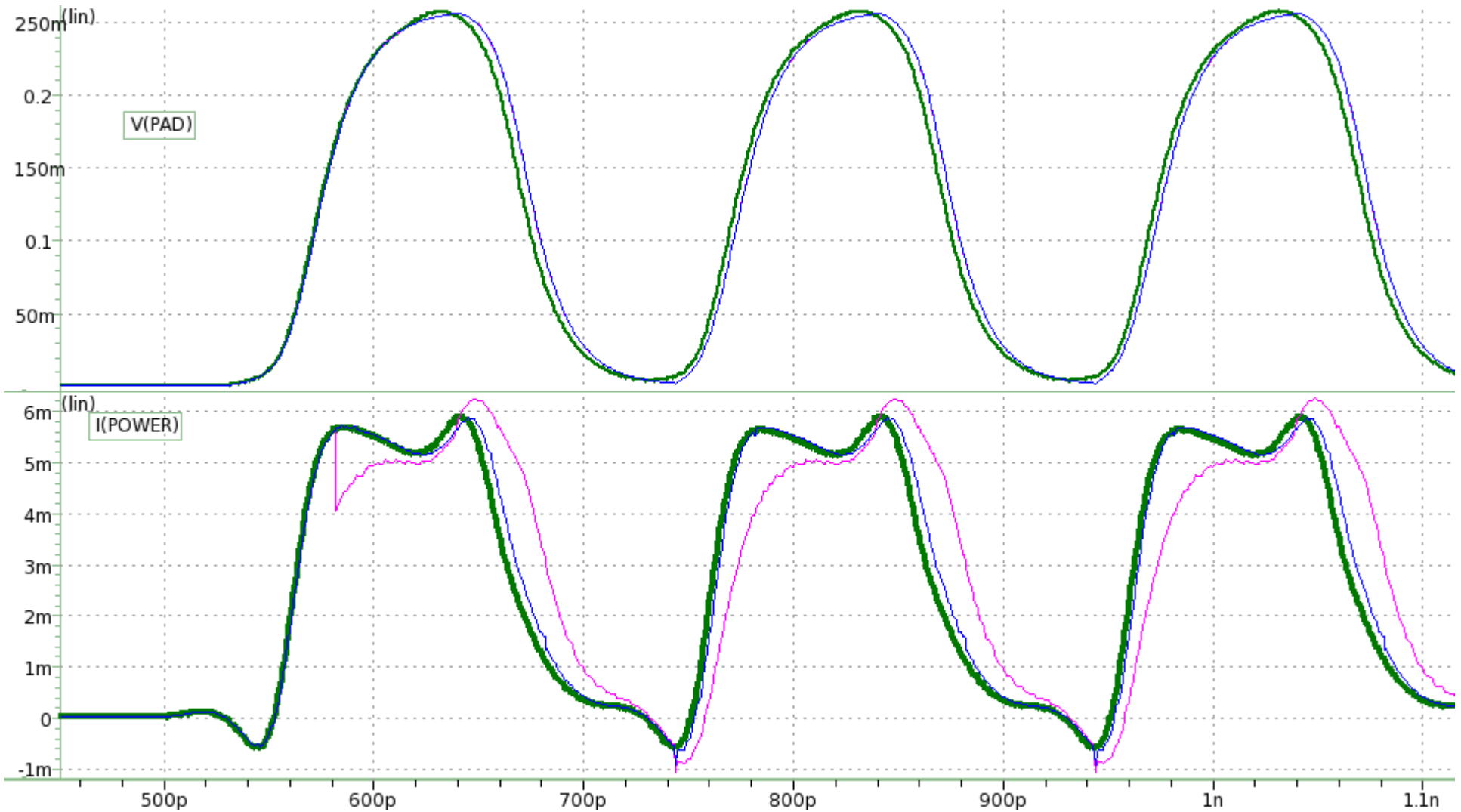
DDR5 IBIS - with 50 ohm load (at a higher datarate)



Transistor Level (TL)
IBIS old
IBIS new

IBIS UI = 319p
SIM UI = 100p (10 Gbps)

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Conclusions

- IBIS power current prediction at overclocked datarates is not optimized as it could be, in current EDA tools
- A superposition technique has been tested to be able to improve the power current correlation between IBIS and Transistor Level in overclocking conditions
  - by using a waveform processing tool
  - by considering a very simple test load
- The enhanced Synopsys IBIS algorithm has been tested with different Micron IBIS models and very generic test loads: the current prediction improvement has been successfully confirmed