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# An accurate IBIS modelling technique for Open Drain Drivers

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# Agenda

1 Introduction

5 Conclusion

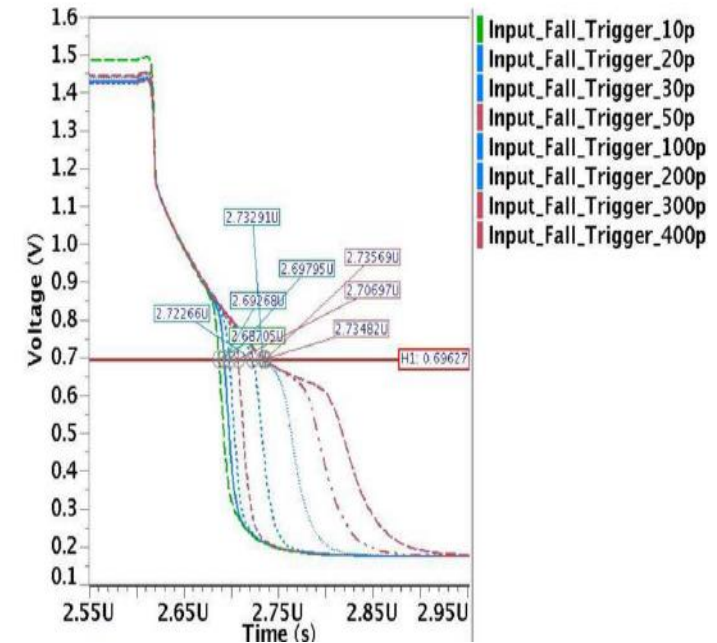
2 Conventional approach

3 Proposed approach

4 Results

## I2C transmitter design challenges

- To meet electrical specification
  - Across wide range of PVT
  - Application requirement to support different combinations of external resistance & bus capacitance ranges
  - Multi-mode support (Standard, Fast, Fast-plus etc.)
- **This led circuit designer to use unconventional approach** (like feedback, controlled drive) to meet electrical specification



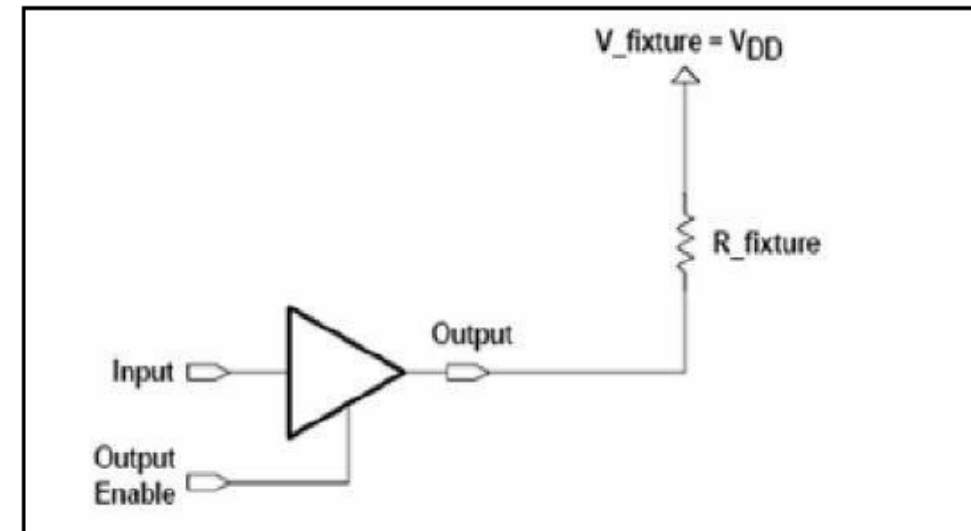
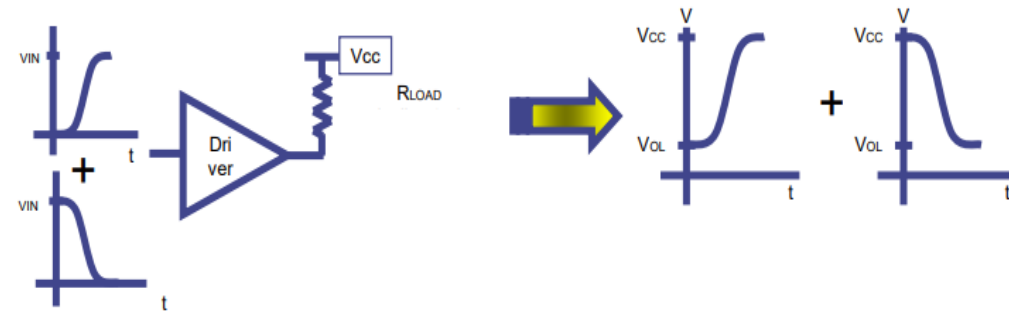
Variation of Fall trigger at N-MOS gate termination due to miller effect

## IBIS development & quality challenge

- IBIS doesn't replicate feedback effect
- Falling trigger of last stage N-MOS gate is dependent on PAD & bus capacitance
- Conventional approach to extract [Rising waveform], [Falling waveform] table is not enough to capture the feedback effect, which results in higher inaccuracy of IBIS vs Spice correlation

# Conventional V-t Data extraction approach

- Open\_drain models have two waveform tables
  - [Rising waveform] : attach external resistance with bus supply and use this load to derive the rising edges
  - [Falling waveform] : attach external resistance with bus supply and use this load to derive the falling edges
- Top I2C cell splits into many sub-models depending upon number of external resistances (under [Model selector])
- I2C transmitter have feedback and so output falling edges controlled by bus capacitance
- **The IBIS model develop with this approach doesn't incorporate feedback effect introduced due to bus capacitance**

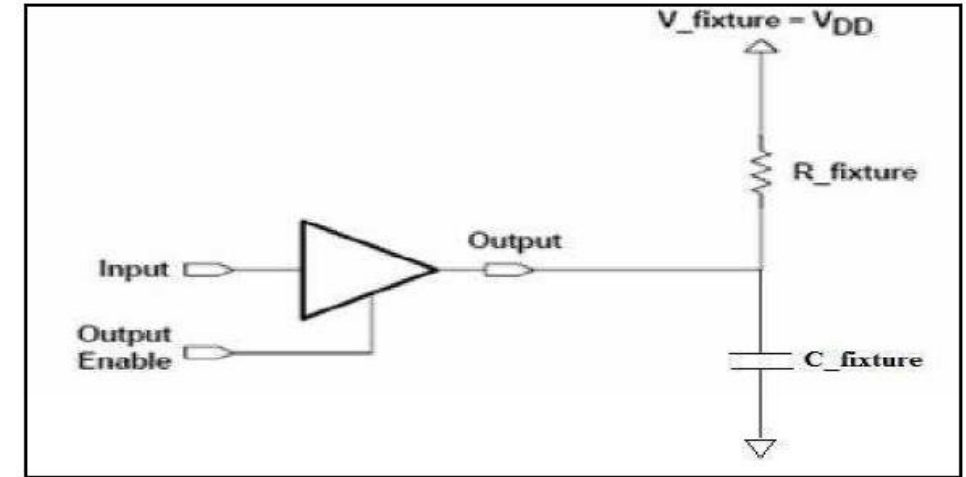


Spice setup for V-T data generation

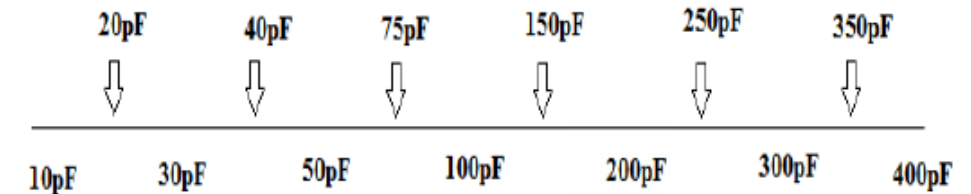


# Proposed approach

- The feedback used in design impacts the effective capacitance and alters the response of the device (Miller effect)
- Higher the bus capacitance, lower impact of miller cap effect is observed
- Top I2C cell splits into many sub-models depending upon number of external resistances along with bus capacitance
  - In order to extract [Falling waveform]  $C_{\text{fixture}}$  is added along with pullup resistance ( $R_{\text{fixture}}$ )
  - $C_{\text{fixture}}$  is selected in such a way that it captures the effect of feedback capacitance for certain range of bus capacitance

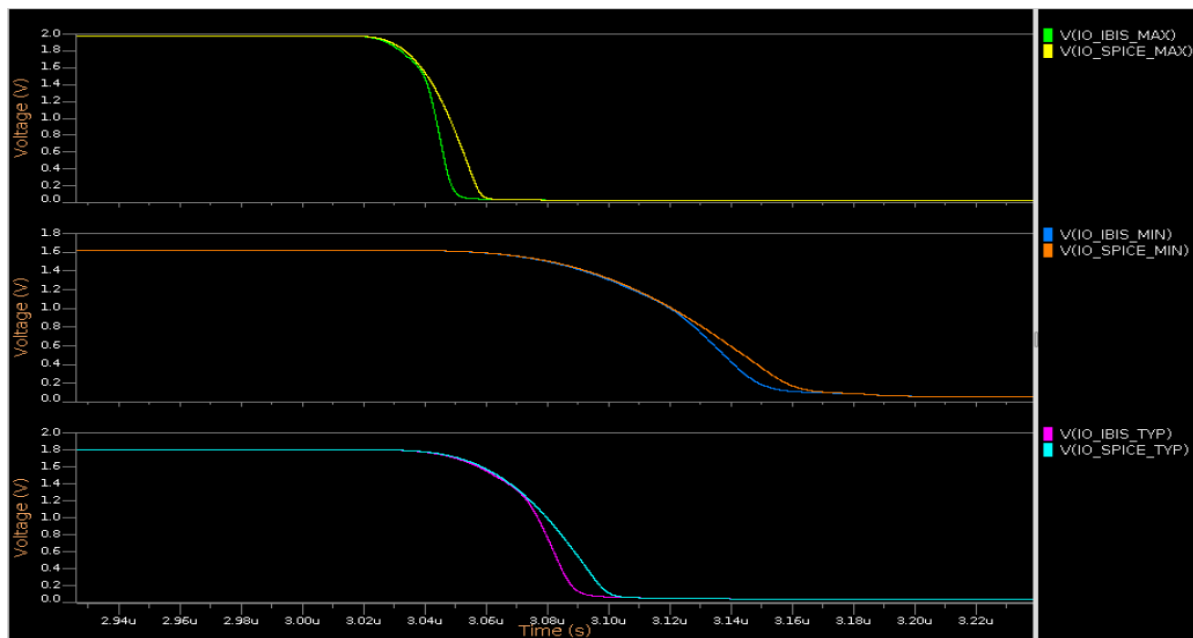


Spice setup for V-T data generation  
(Modified approach).

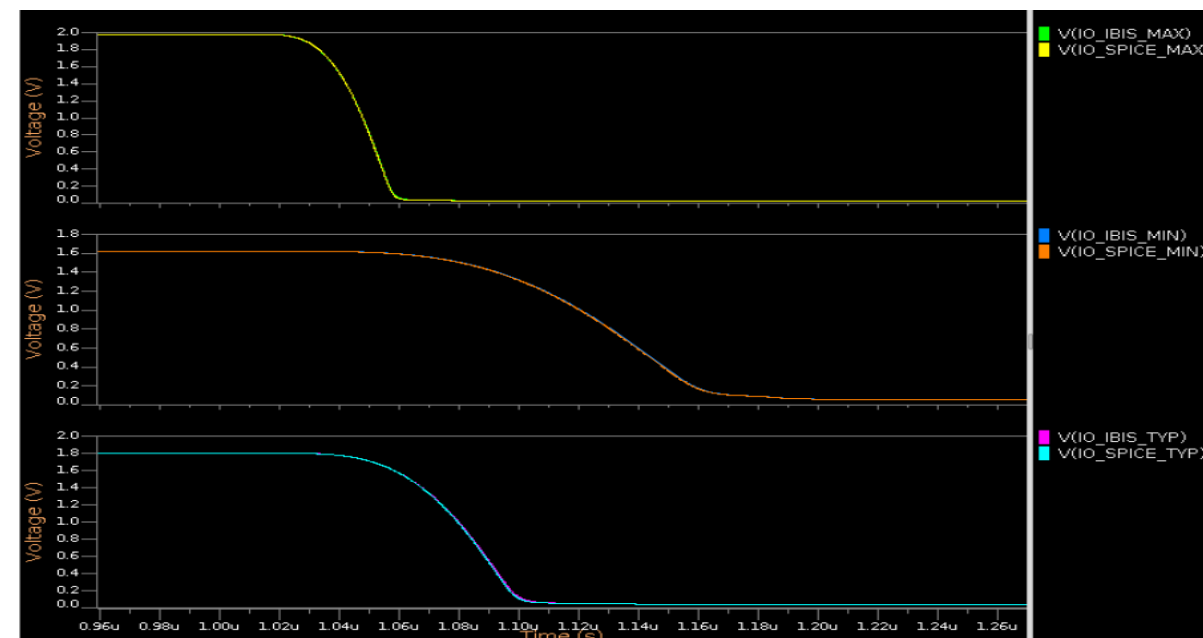


$C_{\text{fixture}}$  selection for V-T data capturing.

# Results



Conventional approach



Proposed approach

Type	Corner	Generic IBIS	Modified IBIS	Spice	% Error Generic approach	% Error Modified approach
Fall time (ns)	Max	4.932	9.767	9.901	50.19	1.35
	Min	25.807	31.165	31.212	17.32	0.15
	Typ	10.828	17.351	17.641	38.62	1.64

Comparison table



# Conclusion

- IBIS vs Spice correlation
  - Proposed approach has very high accuracy (~1%), where generic approach has very significant error(~50%)
- Model development & validation cost
  - higher number of models in proposed approach
    - Automation & parallel computing machines eases in achieving almost same development & validation time
    - Justifiable for such high accuracy
- Approach can be used for any design having feedback from IO's PAD to last stage MOS gate





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