A Novel Simulation Flow for DDR5 Systems with Clocked Receivers

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Outline

- Motivations
- DDR5 Specification and SI
- DDR5 DRAM Device Models
- Clocked IBIS-AMI Time-Domain Simulation
- Advanced IBIS-AMI Flow
- Key Takeaways

Motivations

Demystifying DDR5 SI Simulation

DDR5 Simulations Aren’t Like Before

- DDR5 SI simulations look a lot different from DDR4
  - Equalization, clocking, “stressed eye” mask

- Translate DDR5 specification and DDR5 device models into SI simulation techniques
  - Understand how they lead to increased simulation accuracy

- Breaking down the new terminology around DDR5 and DDR5 SI simulation
  - DFE, Rj, BER, DQS clock tree delay, IBIS-AMI, …

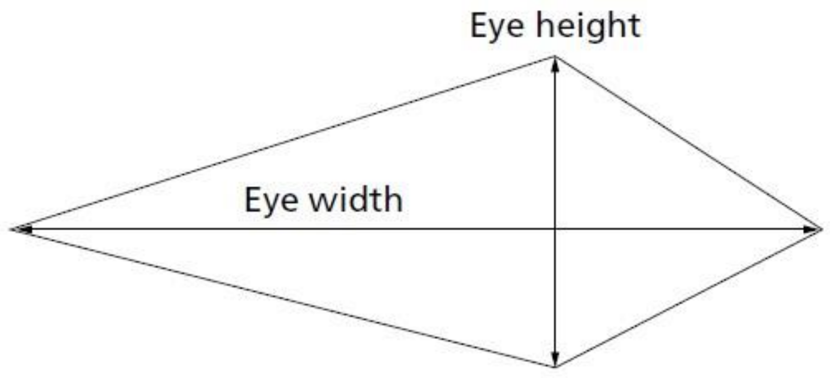
DDR5 Specification and SI

What is the Connection?

DDR5 Stressed Eye

- JEDEC DDR5 specification (JESD79-5B) gives DRAM vendors information to determine if their devices work properly
  - It provides limited information about DDR5 signal integrity
  - It provides no information about SI simulation of DDR5

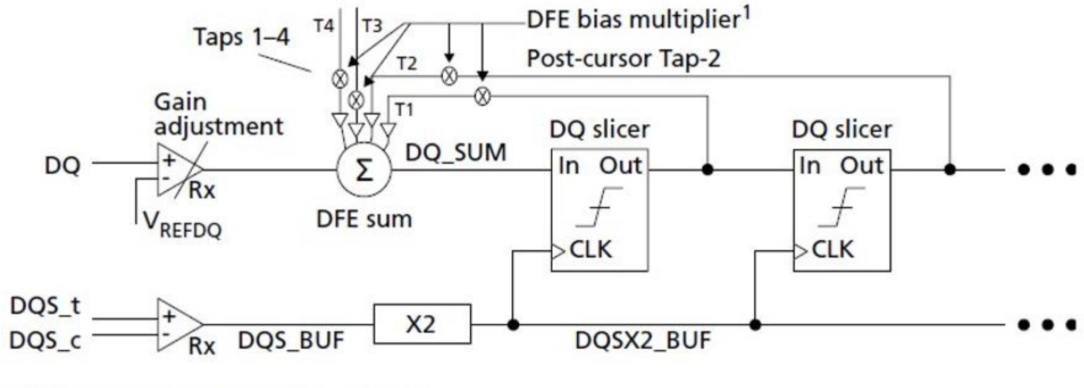
- Section 8.10 introduces Rx Stressed Eye
  - Stressed Eye is a measurement methodology
  - DDR5 specification presents eye height and width as maximums that the device can require for proper operation
  - But from a channel (simulation) perspective, they are the minimum required



DDR5 Receiver Mask

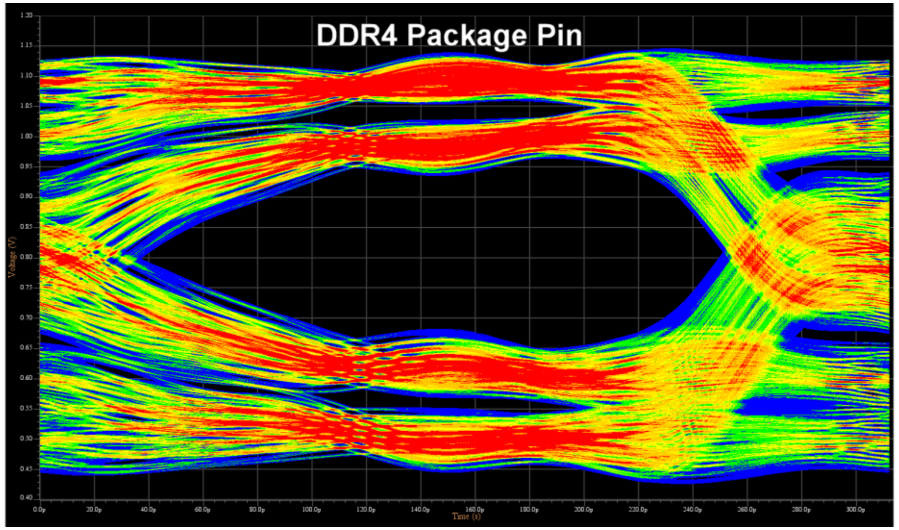
DFE, Evaluation Point, and Clocking

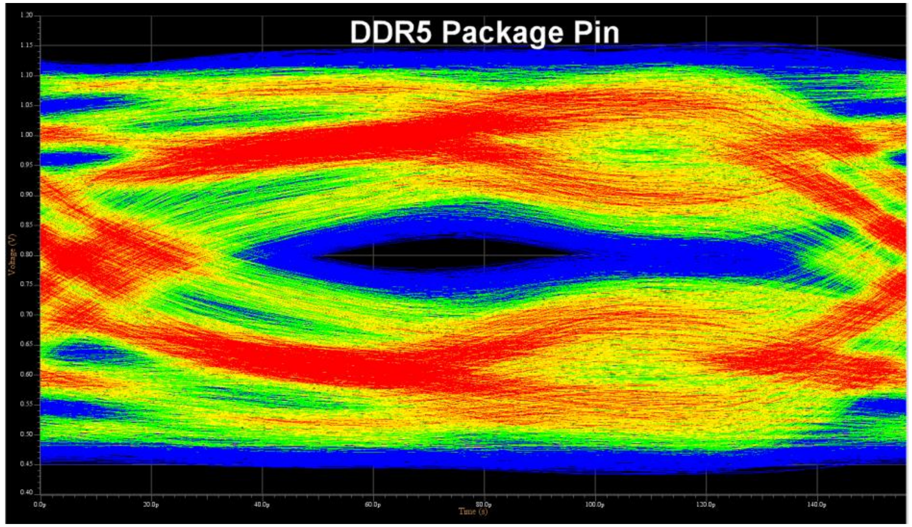
- DFE improves SI for typical DDR5 dominated by ISI
  - This SI benefit comes with increased system complexity
- The signal evaluation point must move inside the DRAM
  - Effects of Rx EQ not seen at DRAM device pin
  - Eye must be constructed at output of summer prior to slicer
- DDR5 DFE is a clocked circuit
  - DQS, the forwarded clock, has a separate physical channel
  - Susceptible to crosstalk and jitter separately from DQ

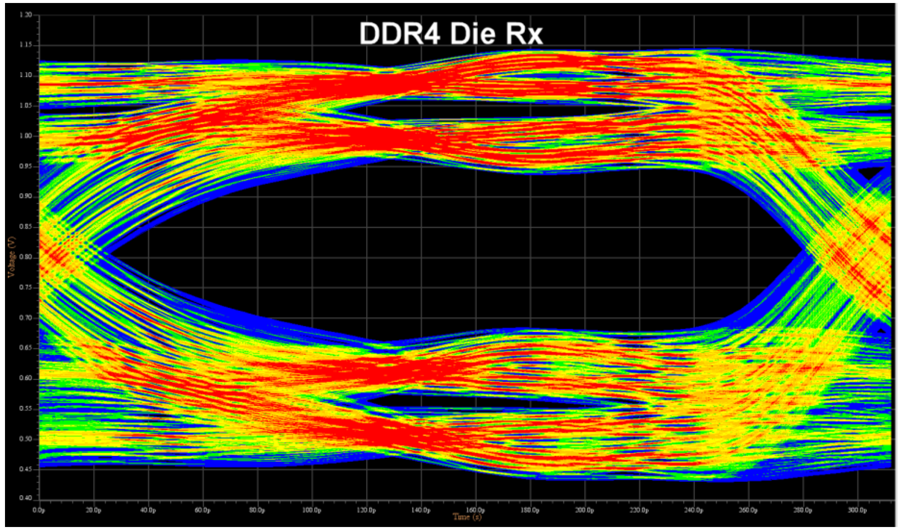


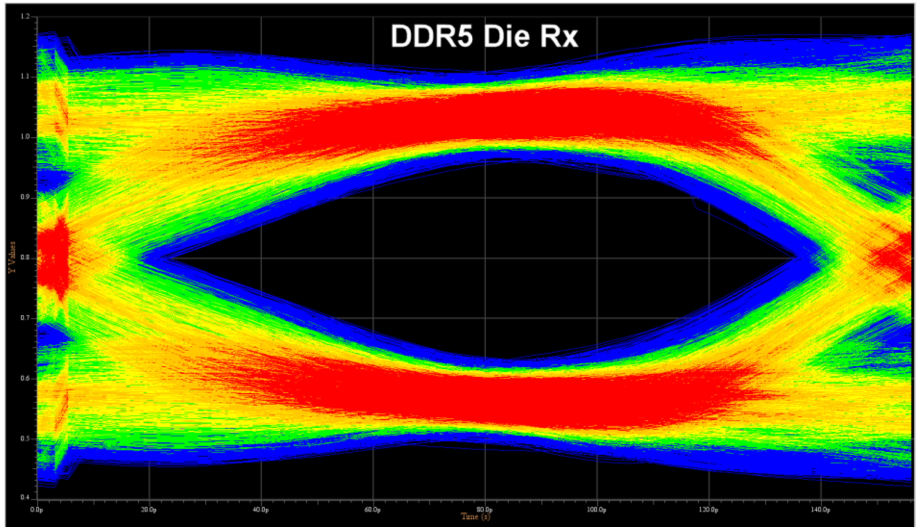
An Example 4-Tap DFE Implementation

Eye Diagram Comparisons for DDR4 vs DDR5



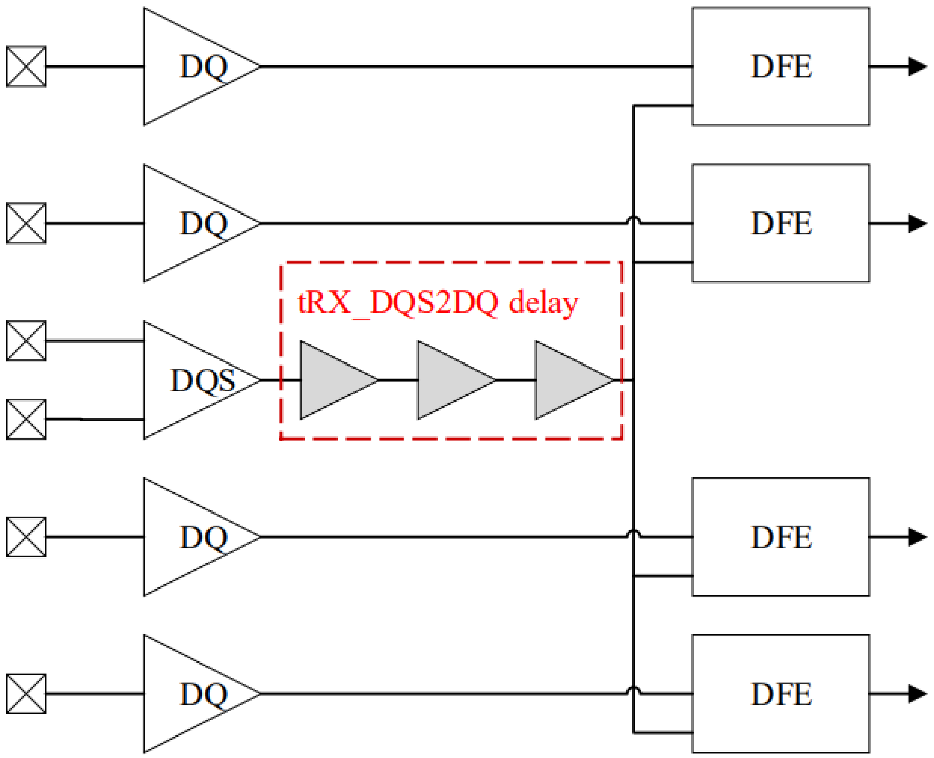






DDR5 DRAM Rx Clock Tree Delay

- DQS is no longer skew-matched to DQ on DRAM die
  - DQS clock tree delay is given by DDR5 timing parameter tRX_DQS2DQ
  - Allowed to be as much as ~3UI delay!
- To compensate, host will launch DQS ahead of DQ
  - Calibration needed to determine exact amount of delay
- Potentially big implications for SI
  - Correlated Tx jitter for DQ and DQS may no longer be aligned once reaching the Rx slicer



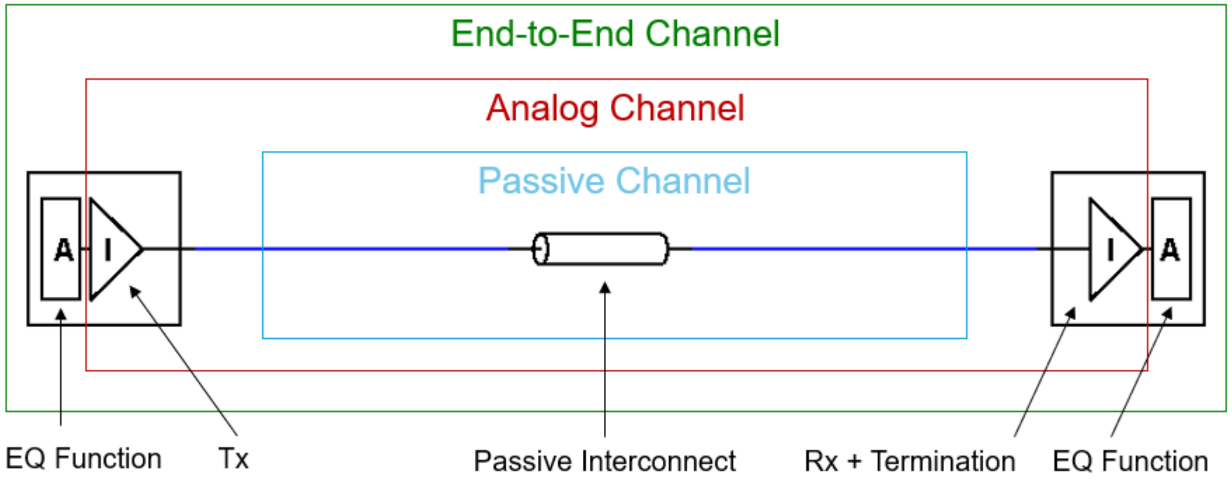
Origin of DQS Clock Tree Delay for DDR5 SDRAM

DDR5 DRAM Device Models

The IBIS-AMI Solution

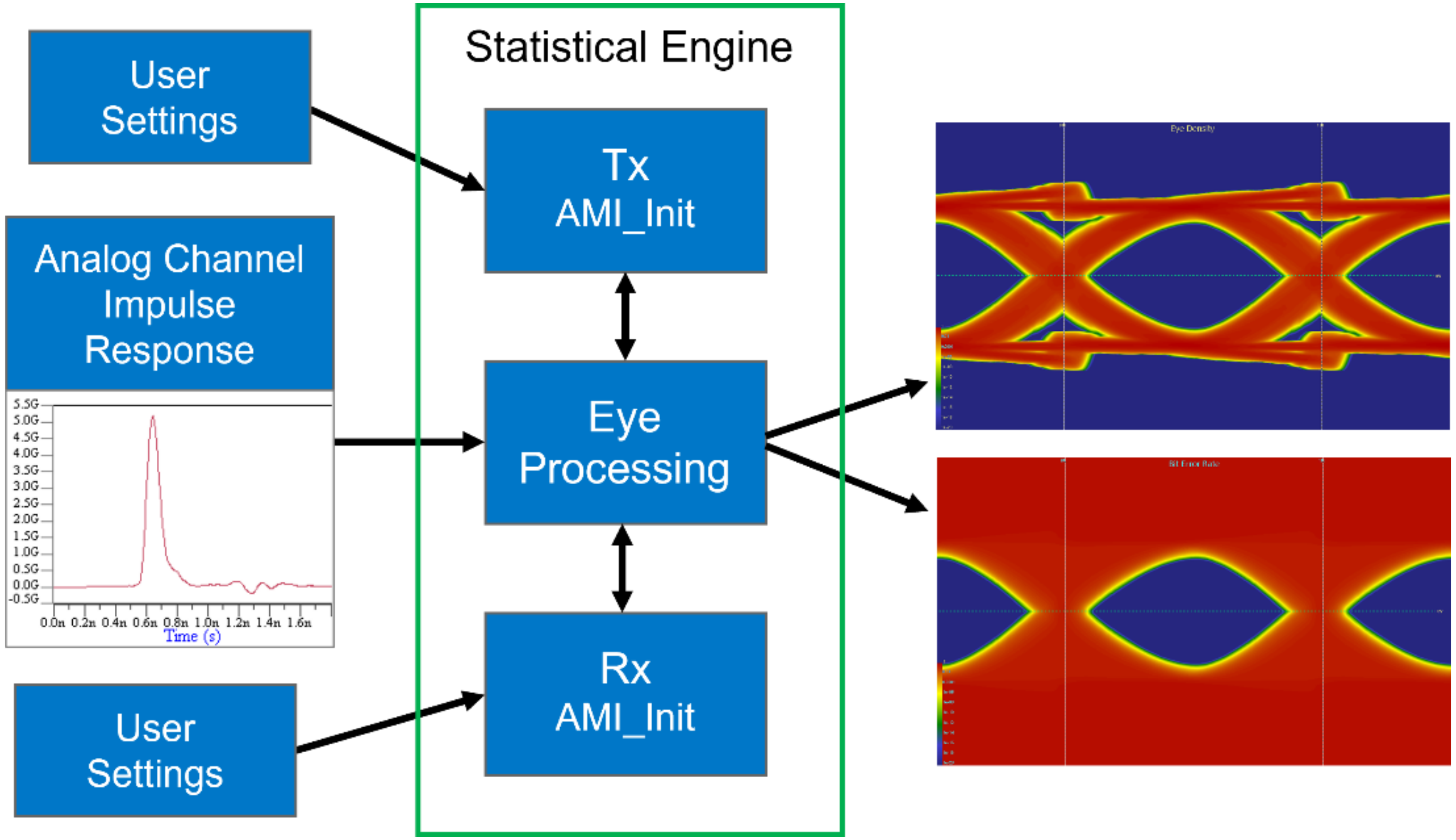
IBIS-AMI Overview

- Traditional IBIS = I-V, Slew Rate, Input Capacitance:
  - Behavioral model based on “observable” characteristics
- IBIS-AMI includes:
  - Traditional IBIS
  - Executable algorithmic model
  - AMI parameter file



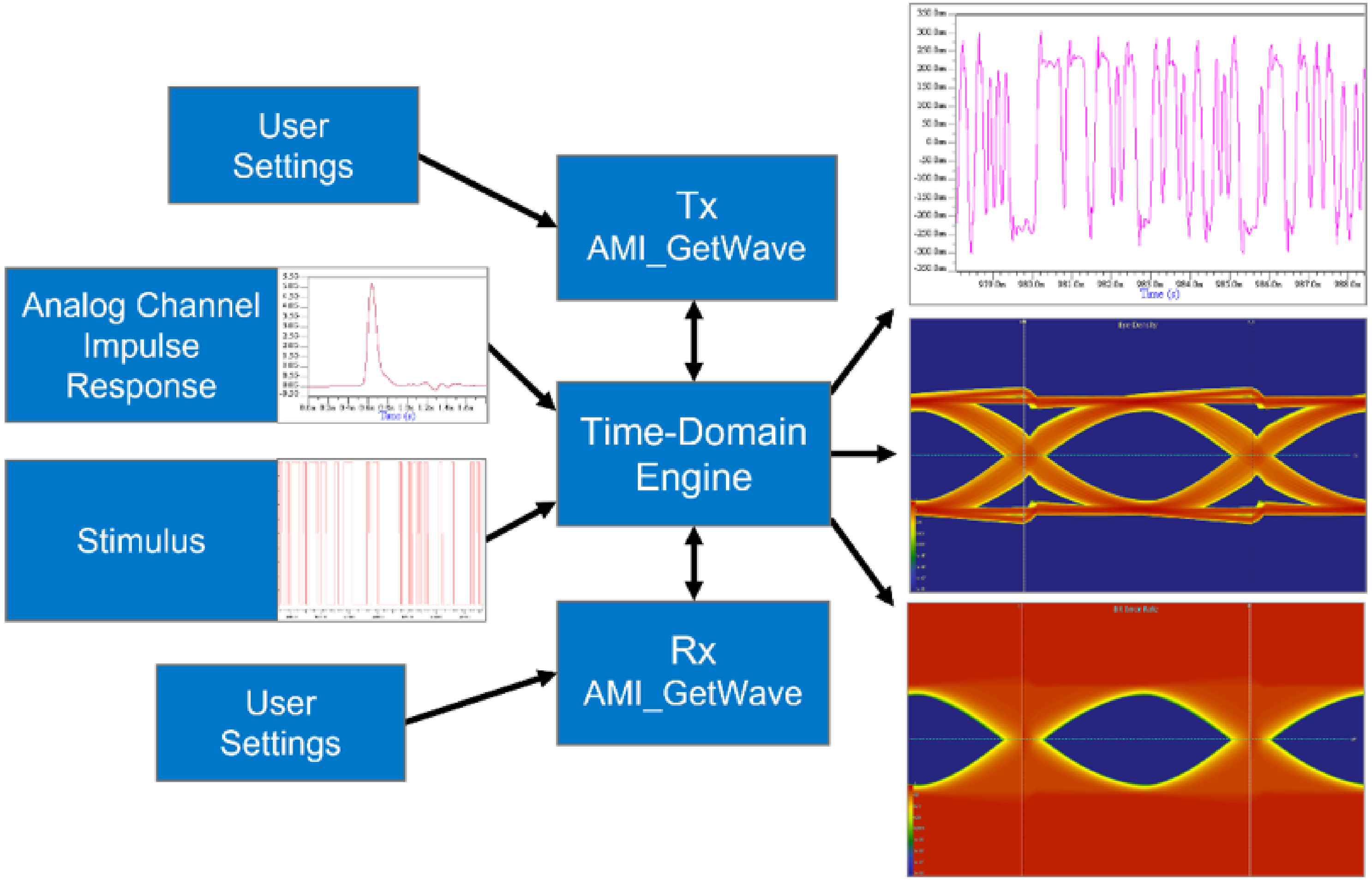
IBIS-AMI Statistical Simulation Flow

- Eye Diagram
  - Generated from superposition of pulse responses
  - Combined jitter PDF of all Tx, channel, and Rx jitter impairments
- Bit pattern
  - No specific PRBS pattern
  - Purely random pattern considered (length determined by EDA tool)
- BER
  - Fast calculation of BER contours to 1e-16 or lower
- Strictly LTI channel



IBIS-AMI Bit-by-bit Simulation Flow

- Not transient simulation
- Ideally generating a waveform input to Rx AMI_GetWave that would match a transient analysis
  - Typically, bit stream processed by Tx AMI_GetWave, then result convolved with channel impulse response
  - Capturing channel non-linearities requires more advanced techniques such as multi-edge response
- Simulate millions of bits in a few minutes
- Add Rx jitter in post-processing



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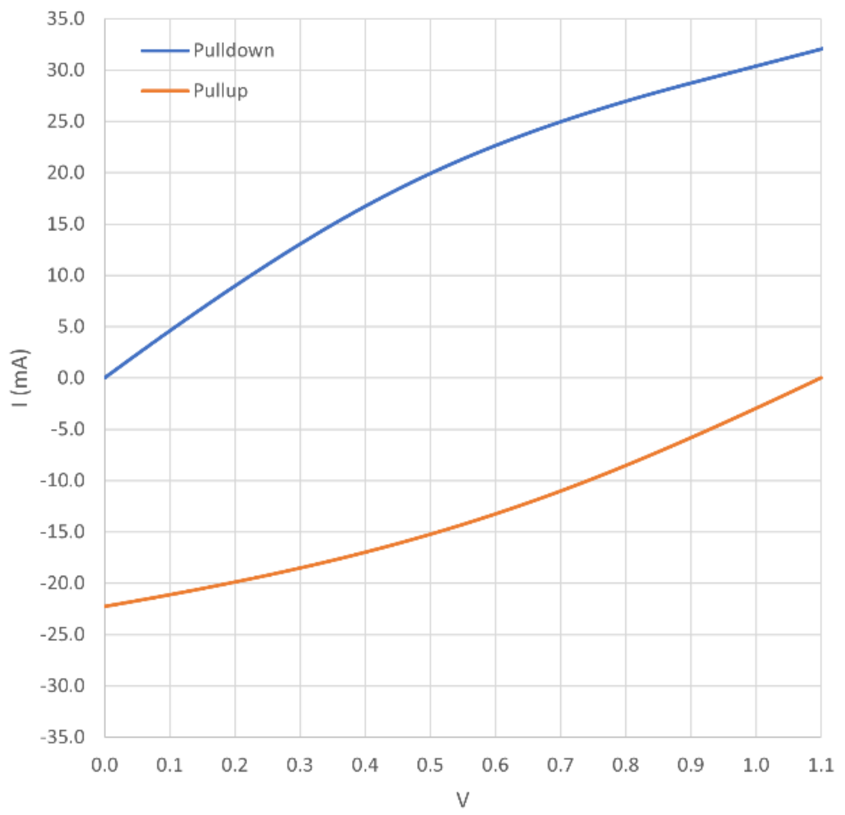
Adapting IBIS-AMI for DDR5

- Simulating single-ended signals with IBIS-AMI presents unique challenges compared to SerDes
- DC common mode voltage
  - AMI Reserved Parameter DC_Offset
- Analog channel non-linearities
  - Tx I-V and rise/fall edge rate mismatch
- Forwarded Clock Architecture
  - AMI Reserved Parameter Rx_Use_Clock_Input
  - Requires AMI model for DQS in addition to DQ
    - Clock times or waveform output
    - tRX_DQS2DQ delay



IBIS-AMI Model Details

- DRAM DQ/DQS Tx
  - .ibs file with I-V, V-t, die capacitance
  - .ami file with jitter parameters (no EQ)
  - .dll/.so are a pass-through (no EQ)
- DRAM DQ Rx
  - .ibs file with I-V for ODT, die capacitance
  - DFE auto-adaptation mode for convenience (not based on real silicon circuitry)
    - Impulse Response based adaptation in AMI_Init function
    - Continued adaptation with LMS algorithm in AMI_GetWave until DFE_Lock time is reached
  - DFE fixed mode for user-based optimization of taps
- DRAM DQS Rx
  - Implements "Wave" and "Times" options for input to DQ Rx AMI model
- Controller IBIS-AMI
  - Tx/Rx architectures not defined by JEDEC
  - Multi-tap DFE expected
  - May include CTLE
  - Possible Tx FFE
  - DQS model could include phase interpolator

Clocked IBIS-AMI Time-Domain Simulation

Implementing Rx_Use_Clock_Input

IBIS-AMI Time-Domain Sim With Clocking

- IBIS 7.1 introduced Rx_Use_Clock_Input
  - Wave or Times uses DQS as forwarded clock
- DQS (Clock) net is simulated first
  - Clock waveform (or zero-crossing times) is saved (2)
- DQ (data) net is second
  - Saved clock waveform (or zero-crossing times) is used during the AMI_GetWave call of the Data Rx DLL (3)
- DQS has its own Tx and Rx AMI DLLs for EQ, jitter, etc.

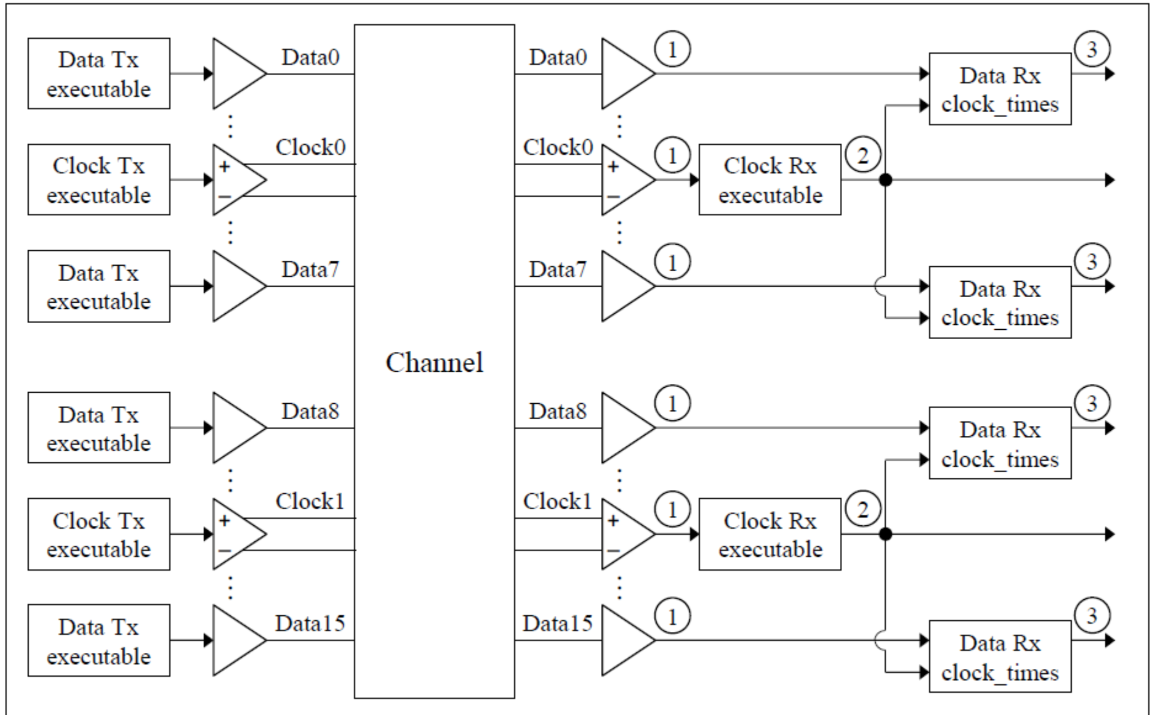
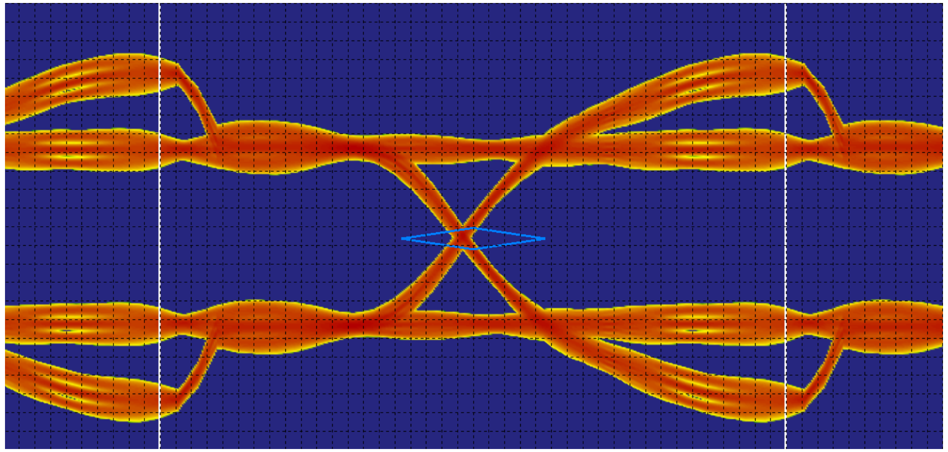


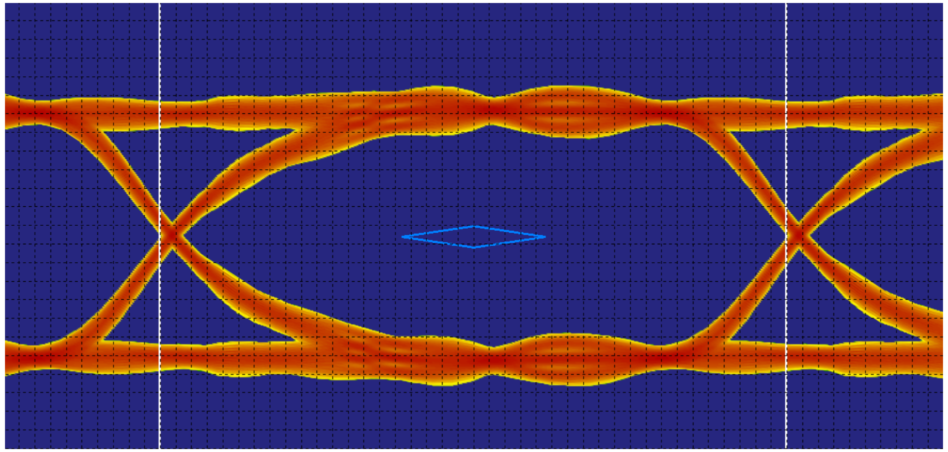
Figure 42 from IBIS Specification (Version 7.1)

Clock Phase Matters

- Ideally, DQS transition is centered within DQ bit period
- Clock phase “baked in” to simulated data waveform
  - Data slicing occurs half UI after DFE action
  - Further, adapted DFE tap values depend on clock phase
- Changes to clock phase affect output DQ waveform
- Clock phase must be correctly determined for accurate simulation results



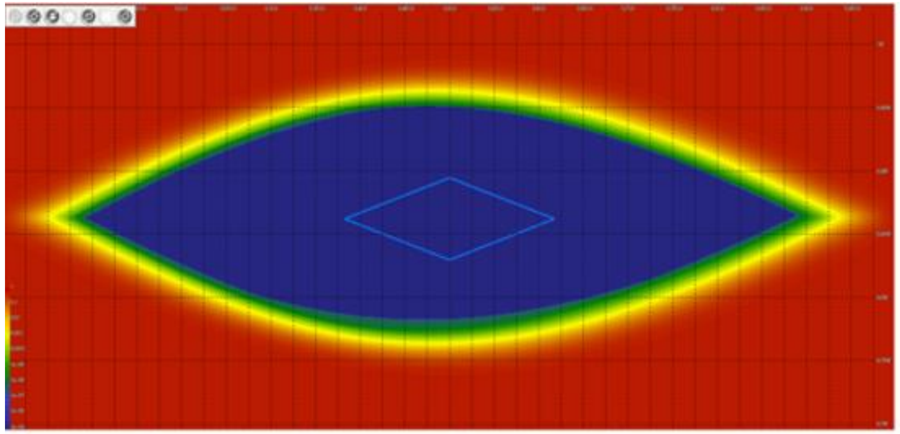
Output data eye diagram with bad clock phase



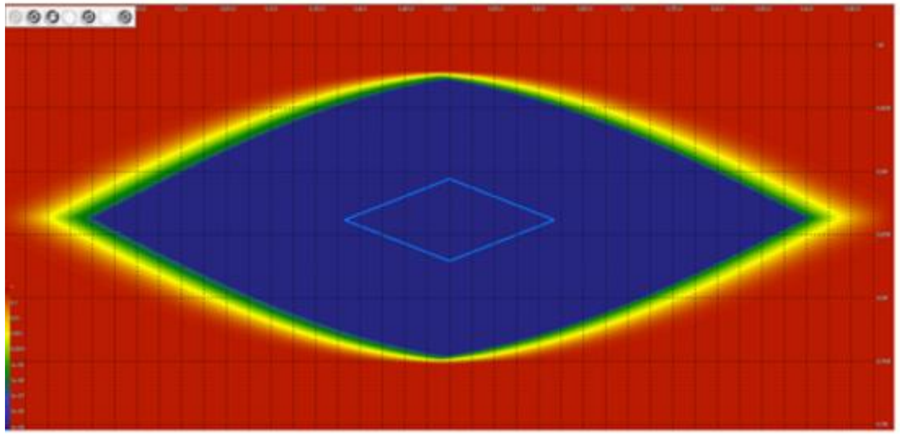
Same input data waveform now with good clock phase

Similar Effect of Jitter on DQ vs DQS

- Clocked DDR5 simulations create eye diagrams that combine the SI effects of both DQ and DQS
- Clocked IBIS-AMI Time-Domain simulation results reveals the similar effect of jitter from DQ vs DQS
  - Timing margin degraded almost identically
- Important to consider the SI of DQS just as carefully as DQ



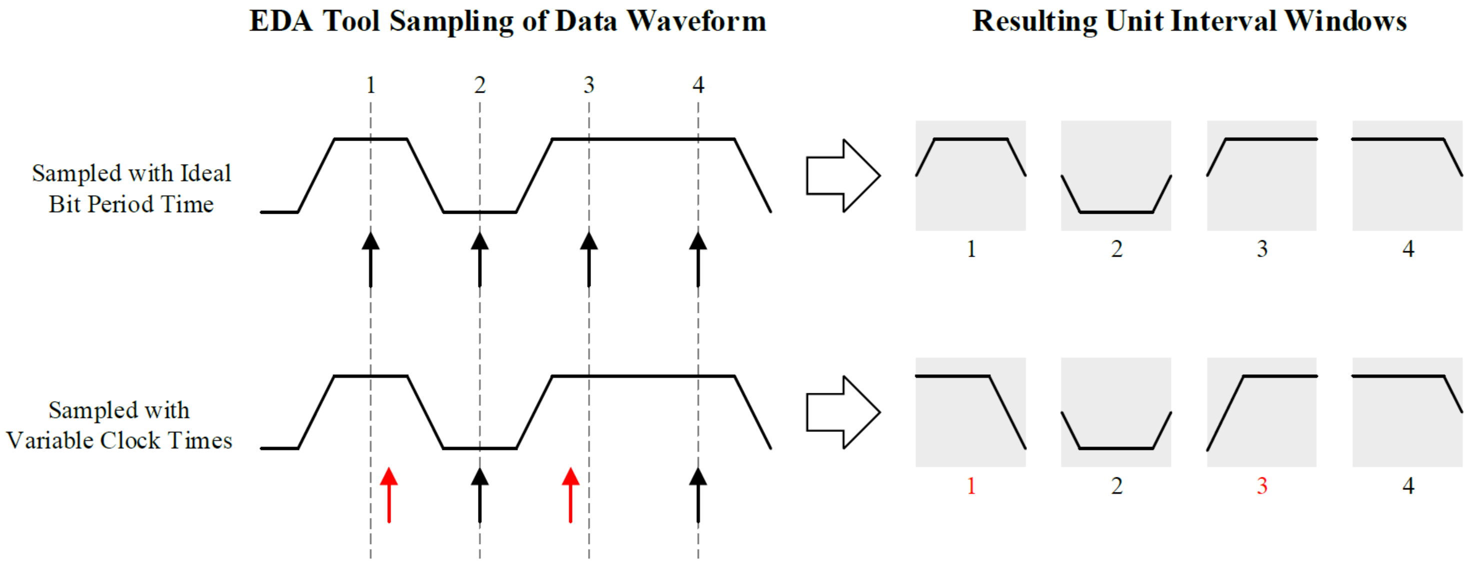
a) BER Plot: DQ is Square Wave with Tx Jitter, DQS is Ideal



b) BER Plot: DQ is Ideal Square Wave, DQS has Tx Jitter

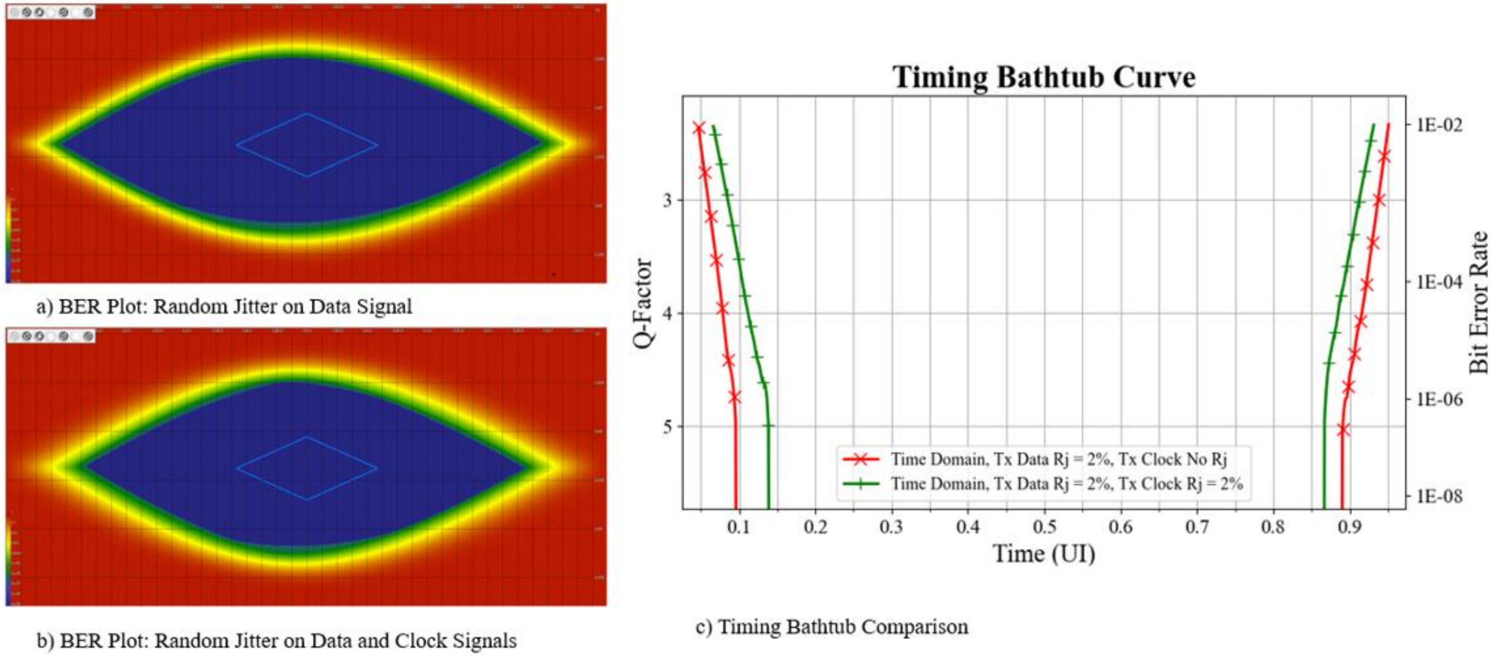
Construction of Simulated DDR5 Eye Diagram

- EDA tool takes a "snapshot" of data waveform around DQS zero-crossing time
  - Snapshot is 1UI in width, +/-0.5UI around the DQS transition time
- The ideal scenario spaces these snapshots every bit period
- When clocking is introduced, jitter creates variation in the zero-crossing times



DDR5 Random Jitter on DQ and DQS

- Random jitter (Rj) is a common jitter source for DDR systems
- Rj can appear on DQ, DQS, or both
- When Rj appears on both DQ and DQS together, the net effect is given by the sum of normally distributed random variables
  - Rj of 2% UI on both DQ and DQS
  - Net effect is ~2.8% Rj in eye diagram



a) BER Plot: Random Jitter on Data Signal

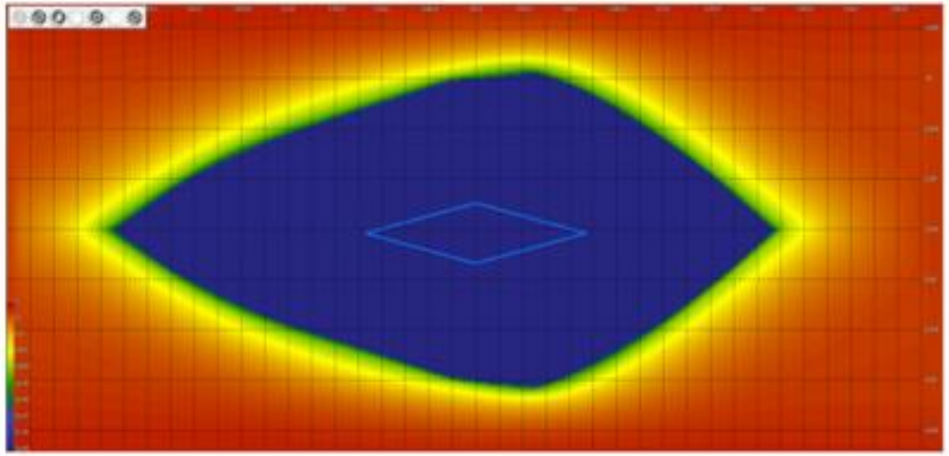
b) BER Plot: Random Jitter on Data and Clock Signals

c) Timing Bathtub Comparison

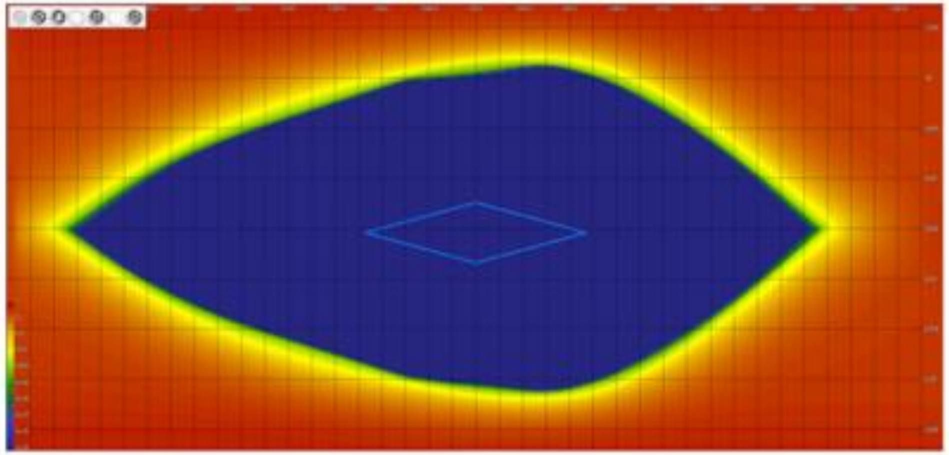
Figure 16: Tx Rj on Data Only Versus Data and Clock Combined

DDR5 Sinusoidal Jitter on DQ and DQS

- Sinusoidal jitter (Sj) is commonly used to model effect of SSN on Tx timing
  - Affects both DQ and DQS
- Because of time delay introduced by tRX_DQS2DQ, there may be significant difference in phase of Sj at DRAM Rx
- For low frequencies of Sj, the effect is self-cancelling
  - Modeling low-frequency Sj on both DQ and DQS provides improvement compared to modeling only on DQ
  - With no significant phase shift, early-arriving DQ is clocked by early-arriving DQS and vice versa



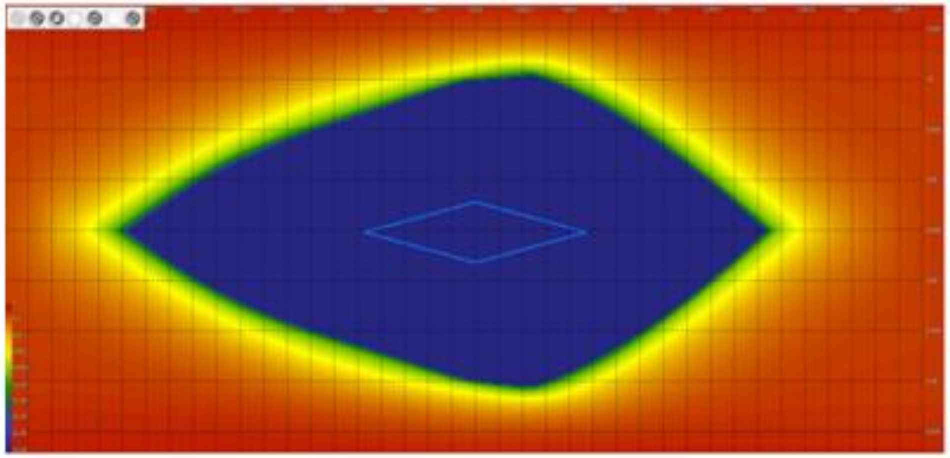
a) BER Plot: Sinusoidal Jitter on DQ Signal Only



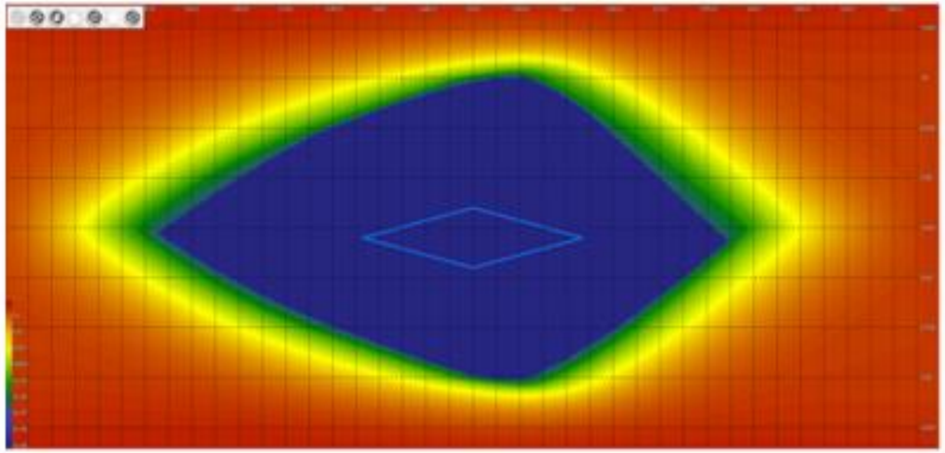
b) BER Plot: Sinusoidal Jitter on both DQ and DQS Signal

DDR5 Sinusoidal Jitter on DQ and DQS

- As Sj frequency increases, effect becomes self-reinforcing
  - Modeling low-frequency Sj on both DQ and DQS provides degradation compared to modeling only on DQ
  - Due to phase shift, early-arriving DQ is clocked by late-arriving DQS and vice versa
- Actual eye diagram results depend on many factors
  - Value of tRX_DQS2DQ (DRAM vendor specific)
  - Magnitude and frequency of Sj (system design specific)



a) BER Plot: Sinusoidal Jitter on DQ Signal Only



b) BER Plot: Sinusoidal Jitter on both DQ and DQS Signal

Advanced IBIS-AMI Flow

Addressing Challenges Posed by Non-LTI Behavior and Low BER Requirements

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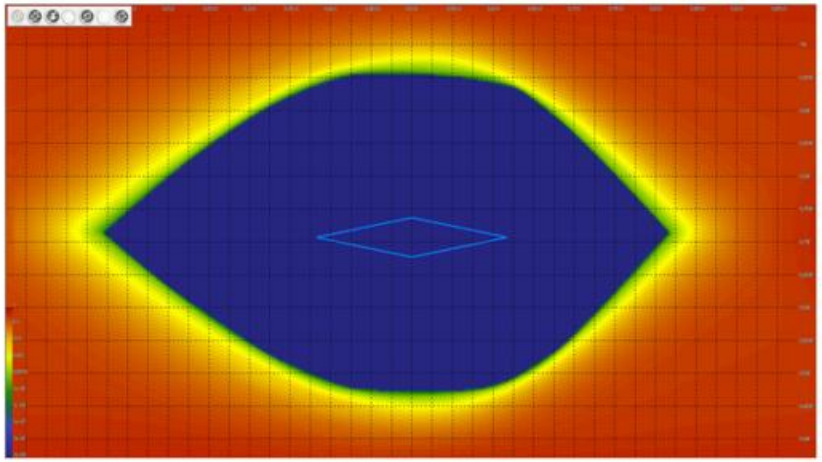
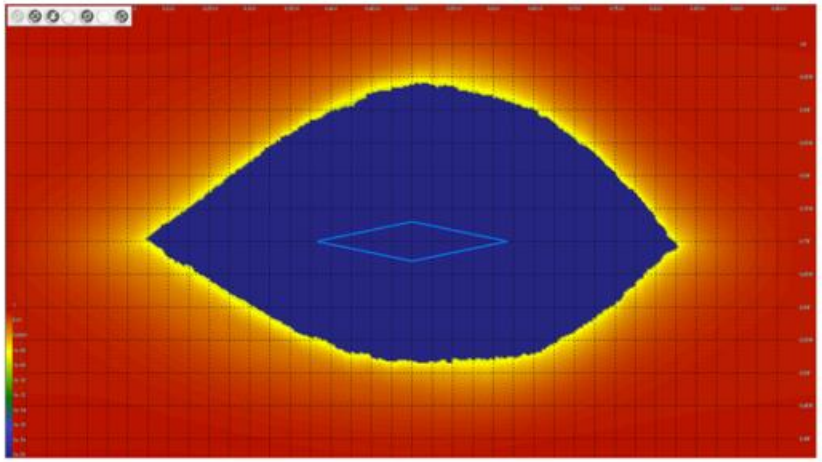
Non-LTI Behavior of DDR5 Channel

- IBIS-AMI Time-Domain flow can only represent non-linear behavior described by AMI_GetWave
- DDR5 analog IBIS Tx and Rx also have non-linear behavior
  - Resulting behavior of system is non-LTI
  - Not modeled by Time-Domain simulation
- An advanced IBIS-AMI flow accounts for these IBIS non-linearities while keeping the AMI equalization
  - LTI-based simulations assume equal swing around Vcenter
  - This symmetry may be not always be accurate representation



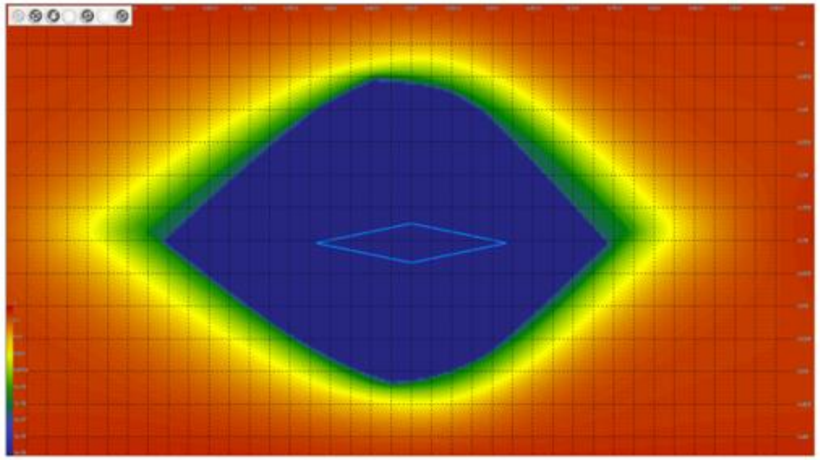
a) BER Plot: Bit-by-Bit Simulation



b) BER Plot: Advanced Simulation

Low BER Requirement of DDR5

- IBIS-AMI Time-Domain simulations running hundreds of millions of bits can reasonably achieve BER down to approximately 1e-8
- DDR5 spec requires evaluating SI at BER = 1e-16
  - Would require simulating at least 10 million billion bits!
  - How to meet BER requirement in practical time constraint?
- An advanced IBIS-AMI simulation uses statistical techniques to achieve BER = 1e-16
  - Unlike IBIS-AMI Statistical flow, advanced IBIS-AMI flow preserves non-LTI effects



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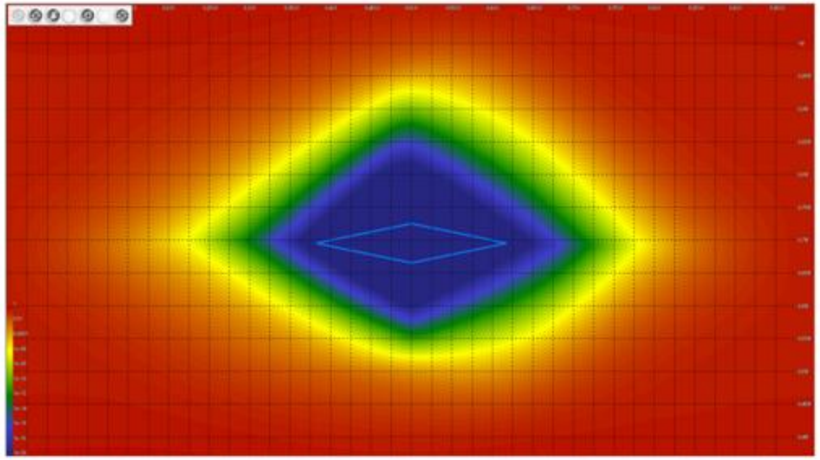

b) BER Plot: Advanced Simulation

Key Takeaways

Key Takeaways

- DDR5 SI simulations are more complicated than DDR4
- Don't confuse DDR5 DRAM device specifications for SI requirements
- The clocked IBIS-AMI Time-Domain flow is a step towards more accurate SI simulation results
  - SI of DQS signal strongly impacts simulation eye diagram
- Non-LTI behavior of DDR5 analog IBIS combined with BER = 1e-16 present challenges to bit-by-bit simulation
  - Advanced IBIS-AMI flow demonstrated which accounts for both effects

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