Touchstone: Immediate and Long-Term Future

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Agenda

- History Touchstone as a File Format
- Compatibility Between Versions
- Challenges: Industry Use and Proprietary Variants
- Per Port Impedance
- A Workaround and a Proposal for Touchstone 2.1
- Plans Beyond Touchstone 2.1
- Questions for the Community
- References

Touchstone as a Format

- Touchstone was a microwave simulator by EEsof, Inc. in the 1980s
 - Later purchased by Hewlett-Packard, and incorporated into Keysight Technologies products, plus others
- Supports use of an ASCII-text file format to represent network data as scattering or "S-parameters"
- The file format was transferred to IBIS Open Forum management in the early 2000s



Compatibility Challenges

- Touchstone 1.0 was never published as a specification or standard
- A draft Touchstone 1.1 specification was developed by IBIS in 2002... but also never finalized
 - The format of the data was untouched
- The first formal, IBIS-approved specification for Touchstone was Touchstone 2.0 in 2009
 - The original Touchstone file format is supported and explained there
 - Defines the official 1.0 and 2.0 syntax

Touchstone® File Format Specification

Version 2.0

Ratified by the IBIS Open Forum April 24, 2009

Two Problems Today

- Touchstone 2.0 is not in widespread use
 - Tools seem to support the format, but actual 2.0 files are rarely seen

- Touchstone 2.0's key feature is available in proprietary versions of Touchstone 1.0
 - Independent impedances declared per port

[Version] 2.0 # MHz Z MA [Number of Ports] 1 [Number of Frequencies] 5 [Reference] 20.0 [Network Data] !freq magZ11 angZ11 100 74.25 -4 200 60 -22 300 53.025 - 45 400 30 -62 500 0.75 -89

Working theory: Touchstone 2.0 does not include the key features customers want, but adds complexity

Per Port Impedance

- Touchstone's reference default is 50 Ω
 - This originates with coaxial cables for RF
 - This is adequate for most PCB interconnect
- For supplies, smaller references are used
 - 0.01 $\boldsymbol{\Omega}$ is the order of magnitude
- Combining signals and supplies into one Touchstone file can cause precision, file size or other issues

How do we provide poweraware Touchstone correctly?



Figure 54 of the IBIS 7.2 Specification

A Workaround and A Proposal

- Touchstone 1.0 supports an option line that includes impedance:
 # GHz S MA R 50
- Touchstone 2.0 adds an optional [Reference] line to override this [Reference]
 - 50 75 0.01 0.01
- Proposed Touchstone 2.1 would allow the following for 2.1 and 1.0 files
- # GHz S MA R 50 75 0.01 0.01

Is this needed? Would this be useful?

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Plans for Touchstone Beyond 2.1

- Discussions ongoing regarding Touchstone <u>3.0</u>
- Key request # 1
 - Provide port naming and orientation information (explicit input and output)
 - Helps automate connections, but less useful for RF
- Key request #2
 - Support pole-residue or other high-compression format
 - Debate: fitting implies equations defined by the specification

Data Challenge

Rate: 24 GT/s bus
Width: 16 lines (s32p)
= 1024 pairs/freq.

Minimum f: 0 Hz Maximum f: 12 GHz Linear step: 10 MHz = 1200 frequencies @ 0.2 - 1.2 KB/pair = 200 - 1400 MB file

Questions for the IBIS Community

- Are these features the most important ones for Touchstone 3.0?
 - If not, which features are most needed?
- Is version control needed for IBIS features that use Touchstone?
 - EMD, IBIS Interconnect, [C Comp Model] can all point to Touchstone files

The IBIS Interconnect Task Group is considering Touchstone 3.0 features – feedback is welcome!

For More Information

- IBIS Interconnect Task Group
 - Meets via teleconference on Wednesdays, 8 AM US Pacific Time
 - Reflector: <u>freelists.org/list/ibis-interconn</u>
 - Documents & Minutes: ibis.org/interconnect_wip/

- References
 - Touchstone 2.0: ibis.org/touchstone_ver2.0/

Thank you!





Backup





Example of Combined Signal and Power													
ŀ	[Interconnect Model] z11b 78b dq ts2					Touchstone 2.0							
	File_ Numbe	TS r of termina	$z11b_78b_dq_ts2.$	ts		8-1	2 places of precision						
	1	Pin ^{I/O}	pin name	A7	I	DM n DBI n TDQS t	DM DBI TDQS						
	2	Buffer I/O	pin name	A7	I	DM n DBI n TDQS t	DM DBI TDQS						
	3	Pin I/\overline{O}	pin name	C2	1	DQ0	DQ						
	4	Buffer_I/O	pin_name	C2	1	DQ0	DQ						
	5	Pin I/\overline{O}	pin name	в7	1	DQ1	DQ						
	6	Buffer I/O	pin name	в7	1	DQ1	DQ						
	7	Pin_I/O	pin_name	D3	Ι	DQ2	DQ						

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21	Pin_I/O	pin_name	C3		DQS_t	DQS	
22	Duffer T/O		~ 2	1		700	
		PTIL_IIGINC	00	1	<u></u> _	520	
23	Pin_Rail	signal_name	VDD		VDD	POWER	
24	Buffer_Rail	signal_name	VDD		VDD	POWER	
25	Pin Rail	signal_name	VDDQ	- I	VDDQ	POWER	
26	Buffer Rail	signal_name	VDDQ	- I	VDDQ	POWER	
27	Pin_Rail	signal_name	VSS		VSS	GND	

[End Interconnect Model]

[End Interconnect Model Set]

Example courtesy Micron as publicly available on the IBIS website

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