Hybrid European IBIS Summit at SPI 2024
Lisbon, Portugal
May 15, 2024

life.augmented

Accurate IBIS Model for IO pads having Floating Rail ESD Architecture

Presenter : Manish Bansal

Authors: Manish Bansal, Mihir Pratap Singh , Rahul Kumar, Raushan Kumar,

STMicroelectronics Pvt Ltd.

Greater Noida, India

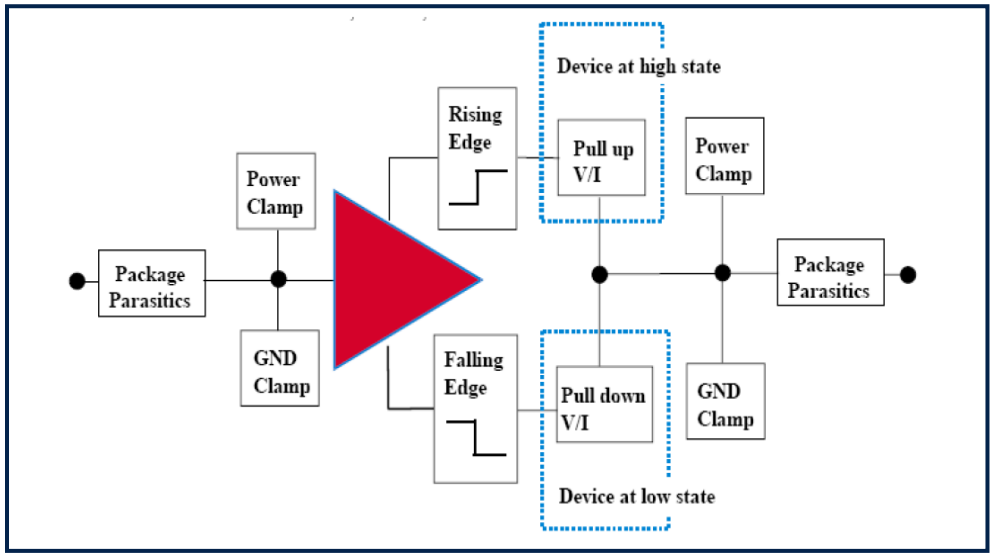
Agenda

1. Introduction
2. About ESD Architectures
3. Problem Description
4. Solution & Results

life.augmented

Introduction

- An IBIS model contains analog behavior of IO pad in terms of :
  - V/I characteristics
  - V/T characteristics
- V/T characteristics contain the transient information for the pull-up/down devices.
- V/I characteristics contain the DC information of pull-up/down and ESD devices.
- Any IO pad has ESD devices to protect it from sudden discharge of current during ESD event.

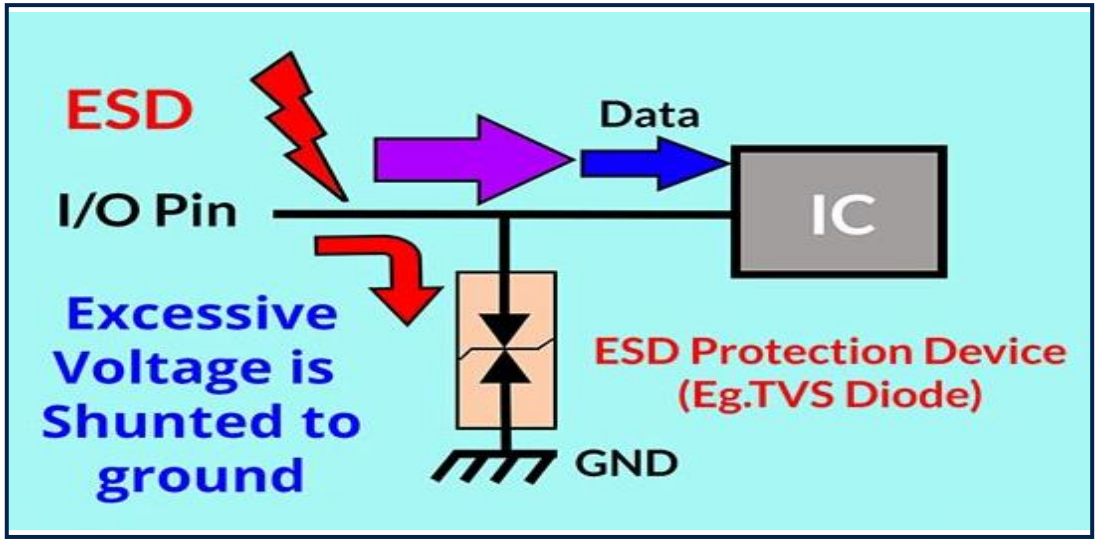


Effectiveness of an IBIS model depends on accuracy of both V/T and V/I characteristics.

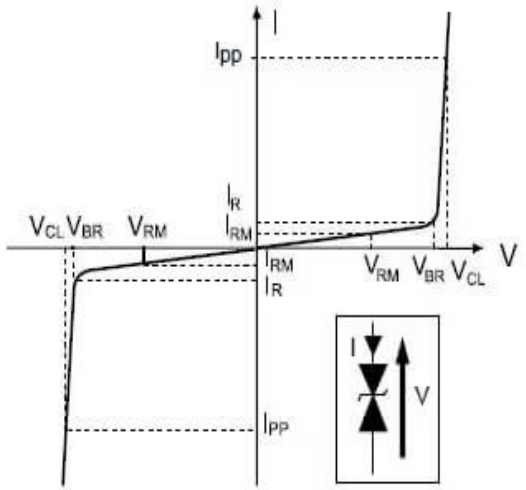
life.augmented

About ESD

- Electrostatic Discharge (ESD) refers to the abrupt release of electric charge from one charged object to another upon contact.
- For integrated circuits (ICs), the substantial peak voltage and current associated with ESD can lead to severe failures.
- In the absence of ESD protection, a high-voltage ESD strike can result in a substantial surge of current directly flowing into the IC, causing damage.



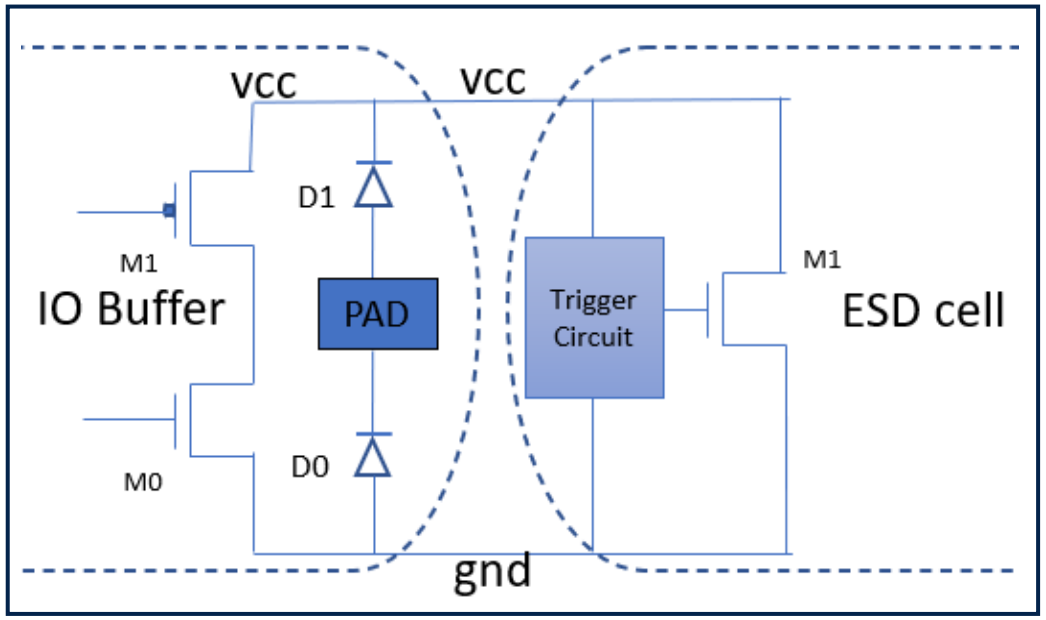
Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_R	=	Breakdown current
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current at V_{RM}
V_{RM}	=	Stand-off voltage
I_{PP}	=	Peak pulse current
R_D	=	Dynamic resistance



life.augmented

ESD Architectures

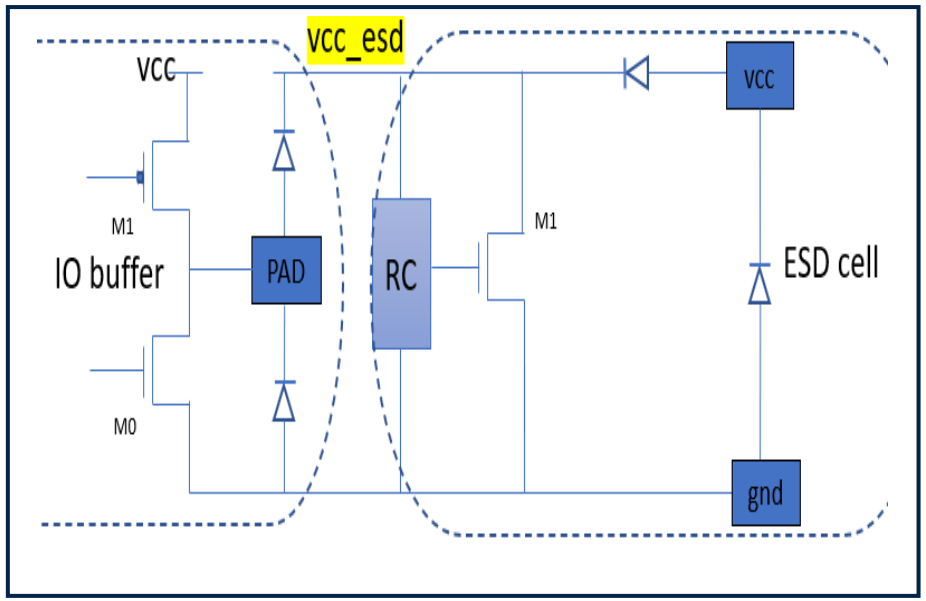
- Choice of an ESD architecture depends on the application of the device.
- It can be classified in 2 ways :
- General Purpose IOs (Non-Failsafe IOs)
  - Standard ESD structure having 2 diodes
  - For negative spikes, diode is placed between IO PAD and Ground rail.
  - For positive spikes, diode is placed between IO PAD and VCC rail.
- Fail-safe IOs
  - These are IOs, where a signal higher than the PAD voltage can occur at the PAD, even when the VCC supply is not present



life.augmented

Floating Rail ESD Architecture for Failsafe IOs

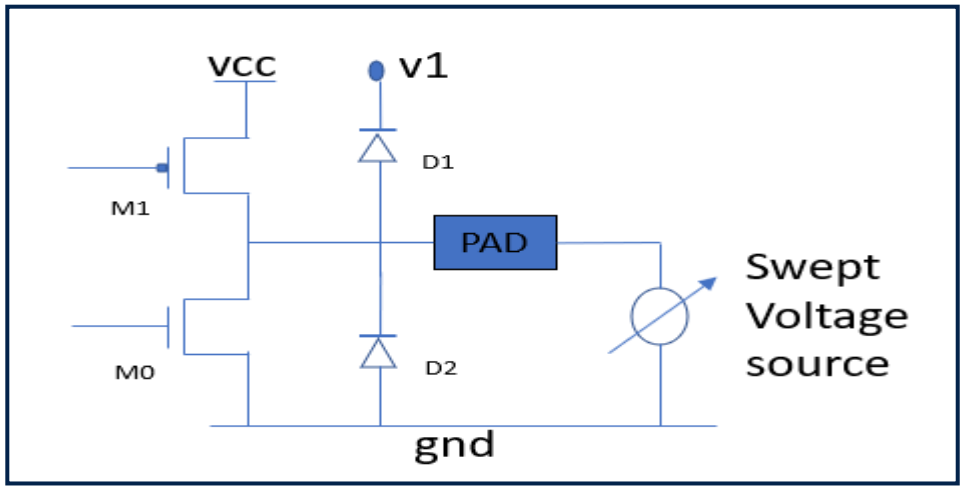
- In this ESD architecture, for negative spikes similar diode is placed between the IO pad and Ground.
- For the positive spikes, diode is placed between IO pad and a floating rail (vcc_esd)
- This vcc_esd is biased using a dedicated ESD cell.
- During the normal operation, range of vcc_esd node is less than normal Vcc.
- During any ESD event, the voltage of vcc_esd will follow the PAD voltage

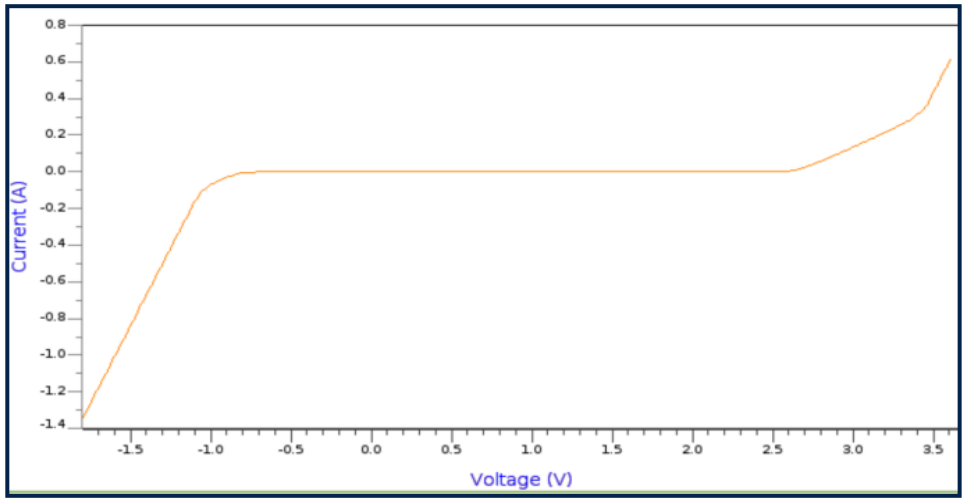


life.augmented

Conventional V/I Data Extraction methodology

- Here v1 node is kept at the same voltage level as VCC.
- The diode D1 will be forward biased when PAD voltage is greater than VCC, causing a high current flow from PAD.
- This works well for non-failsafe IOs
- But this is against the concept of floating rail architecture, where the power clamp diode (D1) is never forward biased.
- This high current will lead to inaccurate IBIS model causing ineffective SI analysis.

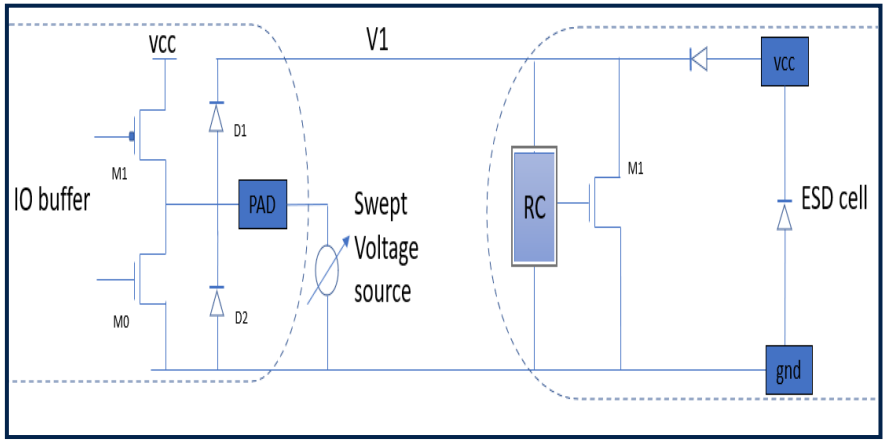




life.augmented

Proposed methodology

- Proposed methodology is to connect the V1 with the actual ESD cell, that will bias this rail.
- Since V1 is a floating node, this will follow PAD voltage when it is swept from +vcc to +2*vcc. Hence diode D1 is never forward biased
- This results in accurate V/I table and hence SI analysis.



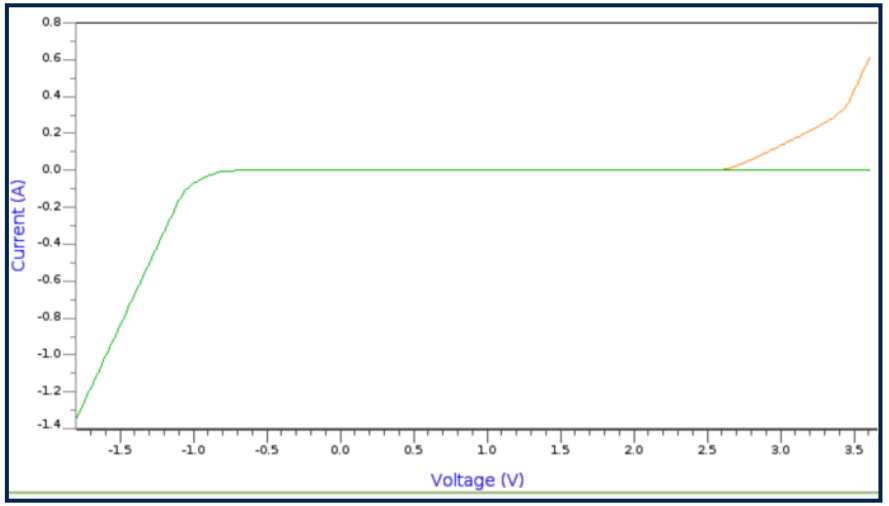


TABLE I. MAXIMUM CURRENT FOR TYPICAL PROCESS @25C

	Conventional Methodology	*Proposed Methodology*
Power clamp Current	616.40mA	2.94pA

life.augmented

Thank you

© STMicroelectronics - All rights reserved.
The STMicroelectronics corporate logo is a registered trademark of the STMicroelectronics group of companies. All other names are the property of their respective owners.

life.augmented