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Accurate SI Analysis under Overclocking conditions with Power-Aware Buffer Models

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Remembering Michael Schaeder

- This work was initiated by our colleague Michael Schaeder
- He worked for more than 25 years in the area of component/buffer modeling, mostly based on IBIS
- We want to share our approach to a common problem called *Overclocking* of IBIS buffer models

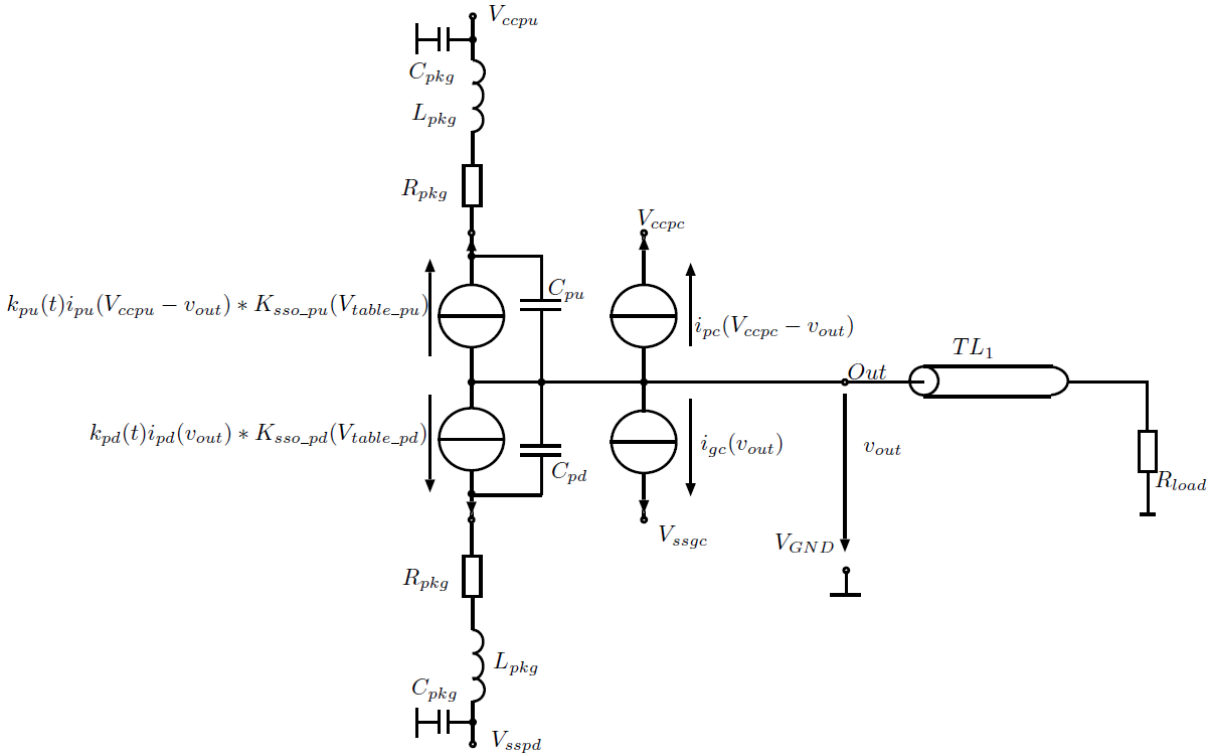
Overview

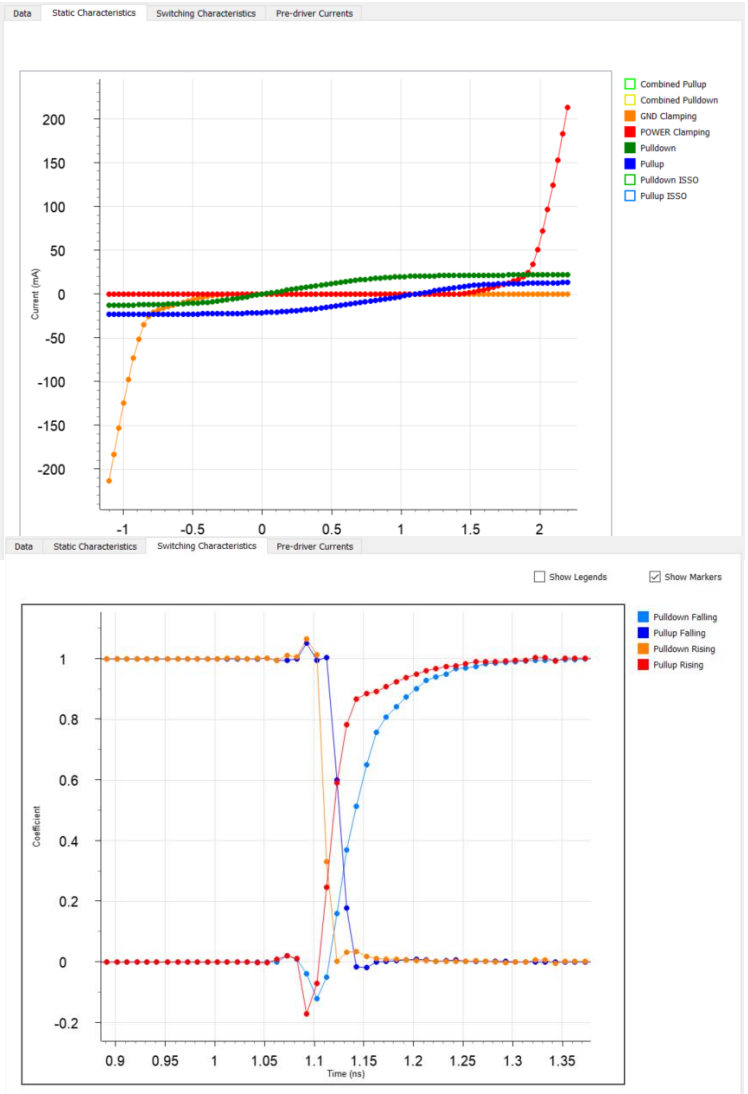
- Introduction:
  - Output Buffer Modeling
  - What is Overclocking?
  - Effects of Overclocking
- Dealing with Initial Delays
  - Considering power-aware buffer models
- Dealing with Overclocking
  - Switching characteristics
- Results
  - Time-domain charts
  - Eye Pattern

  } Comparisons with Reference Tool
- Summary

Modeling the IBIS Output Buffer Behavior

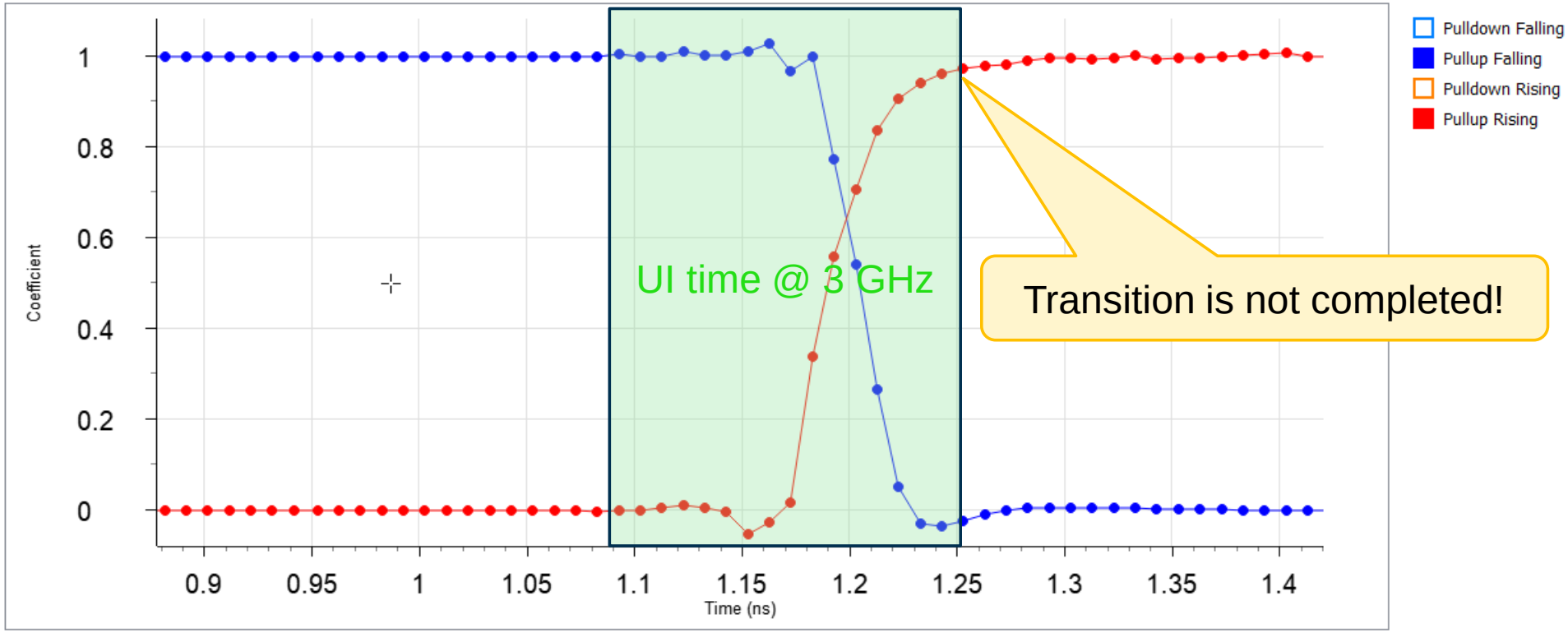
- An output buffer can be modeled by a set of current sources i(t, v)
  - Current sources are functions of output voltage and switching coefficients vs. time
    - These are given in or based on IBIS data





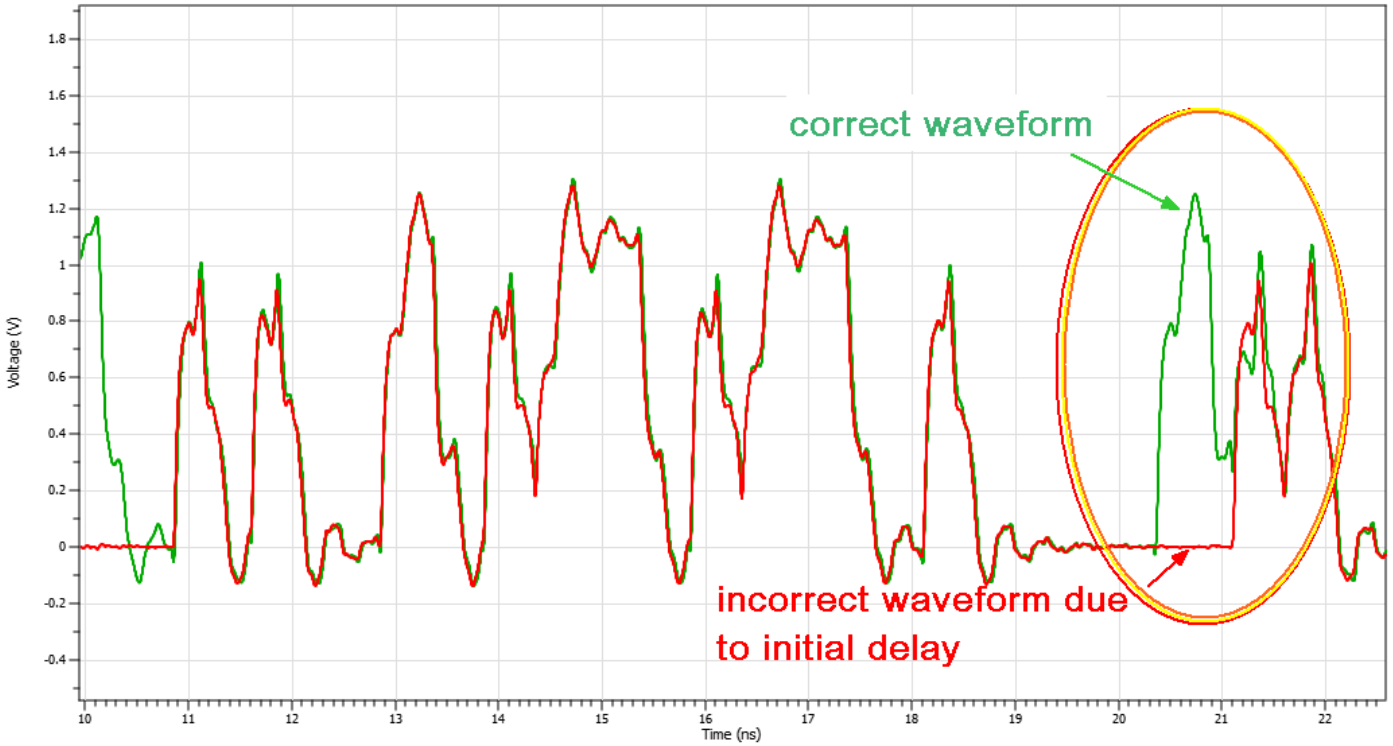
What is Overclocking?

- *Overclocking* happens when an IBIS driver model is operated faster than its switching characteristics would usually allow, i.e. they take longer to switch than the unit-interval (UI) time
  - IBIS assumes to always fully switch from L→H and H→L, using the complete switching characteristics



Effects of Overclocking

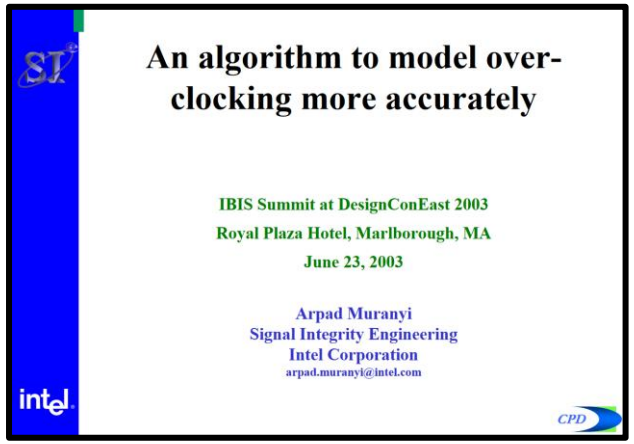
- Simple point-to-point topology, lossy TLs
- Driver model operates in overclocking mode
  - Signal @ Driver Die w/ and w/o initial delay corrections from IBIS simulation
  - Pseudo-random bit pattern @ 1GHz

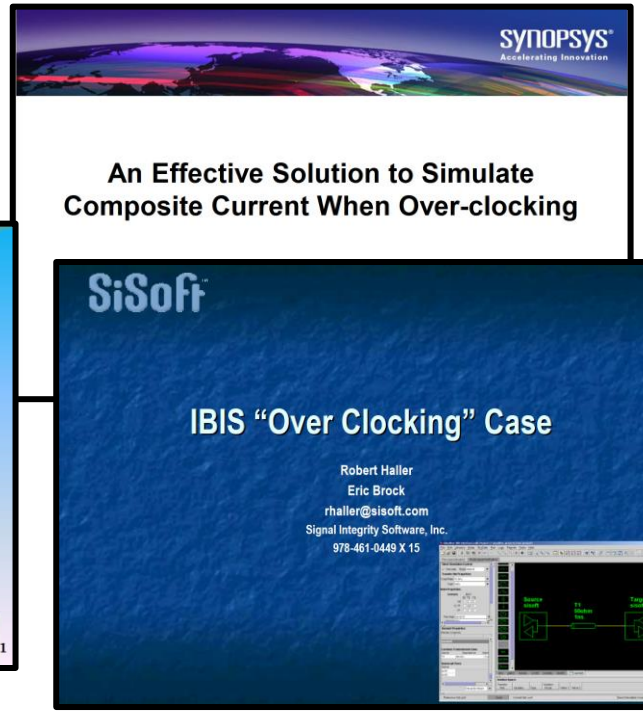


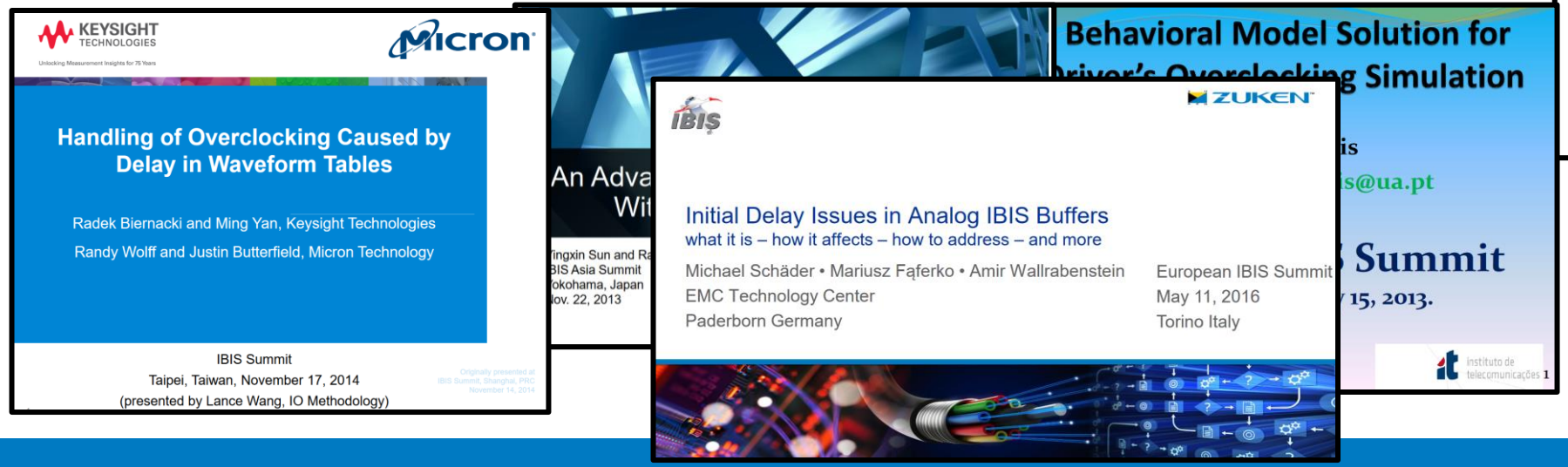
*Note: waveforms are aligned to eliminate delay

Discussing Overclocking

- How to resolve the overclocking issue was discussed already in 2002
- EDA Tool vendors provided several solutions
  - Windowing switching characteristics
  - Overlap multiple switching cycles
- With IBIS V5.0 (power-aware buffer models) additional trouble appeared
- IBIS BIRD 168.1:“Handling of Overclocking Caused by Delay in Waveform Data” → BIRD 177 → [`Initial Delay`] in IBIS V6.1



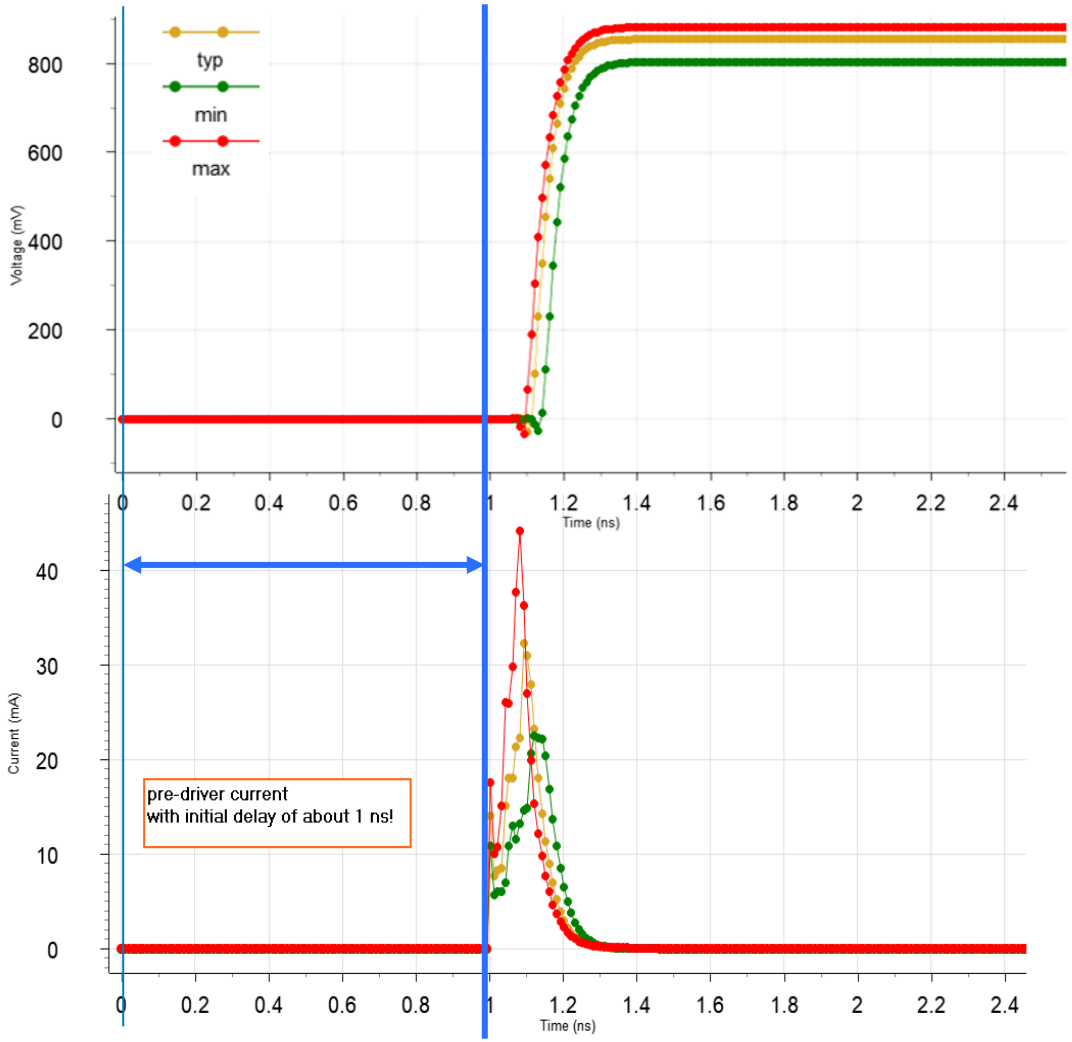




Dealing with Initial Delays

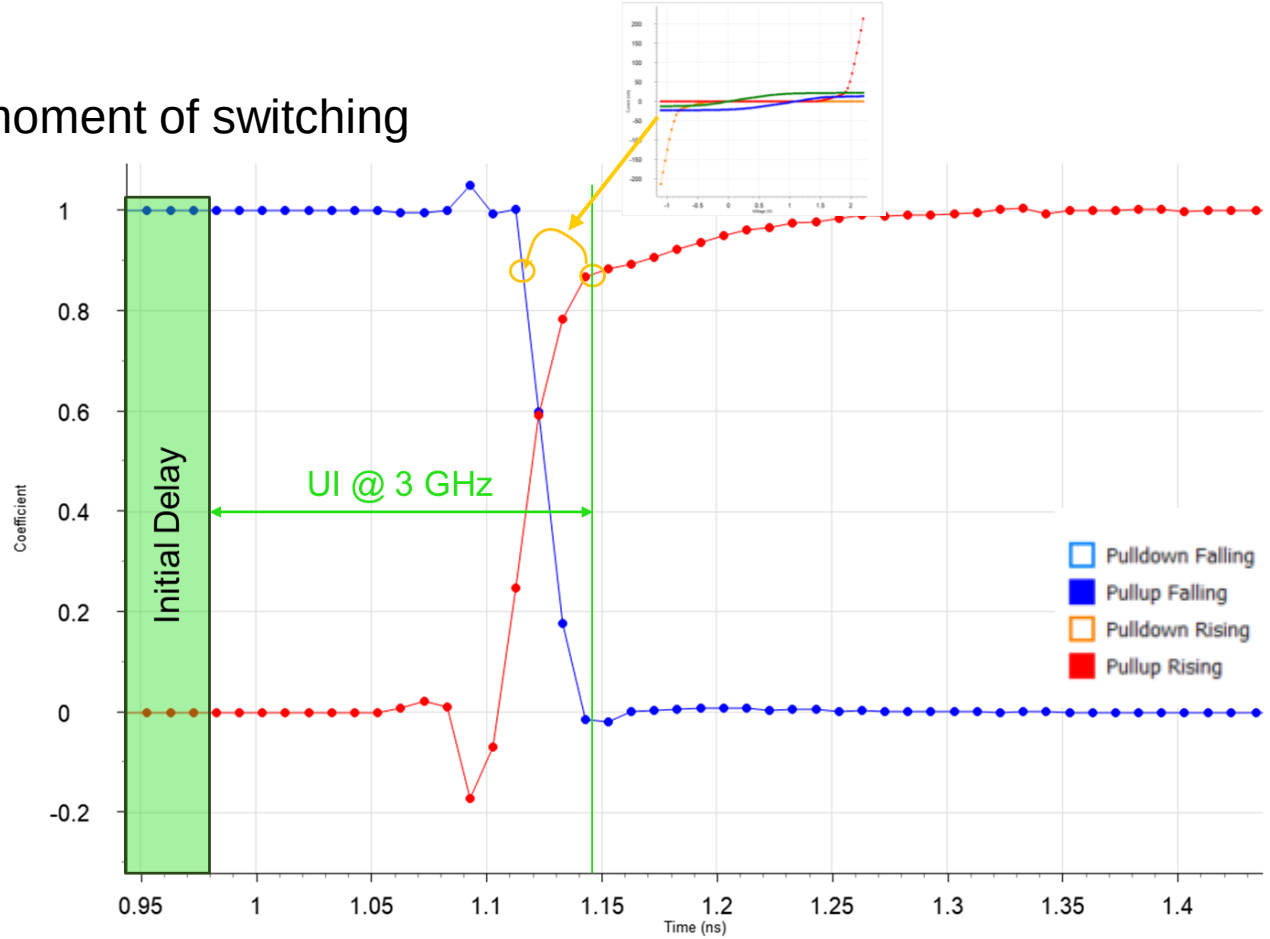
- IBIS data from various vendors show some significant initial delay in the switching characteristics and composite currents
- To describe the actual timing of a buffer, any *artificial* initial delay has to be removed
  - if [**`Initial Delay`**] is given in the IBIS data → use it!
  - Determine the longest possible initial delay from the charts v(t)- and i(t)
    - Composite current i(t) is available for power-aware buffers, only
  - Removing the determined initial delay from v(t)- and i(t) characteristics
    - Keeping the correlation between v(t) and i(t)

→ Derive switching coefficients k(t) from v(t)-, i(t)-, v(i)-characteristics for the output buffer model



Dealing with Overclocking

- When transition is incomplete, the starting point for the next UI needs to be determined
  - At the moment of switching L→H / H→L:
    - Ensuring continuity of the output voltage in the moment of switching
    - Determine currents in all model branches from V/I-tables
    - Determine starting point of the next transition from switching coefficients of the opposite edge
    - Compute next step in time for the output voltage from all current sources and circuit elements of the buffer



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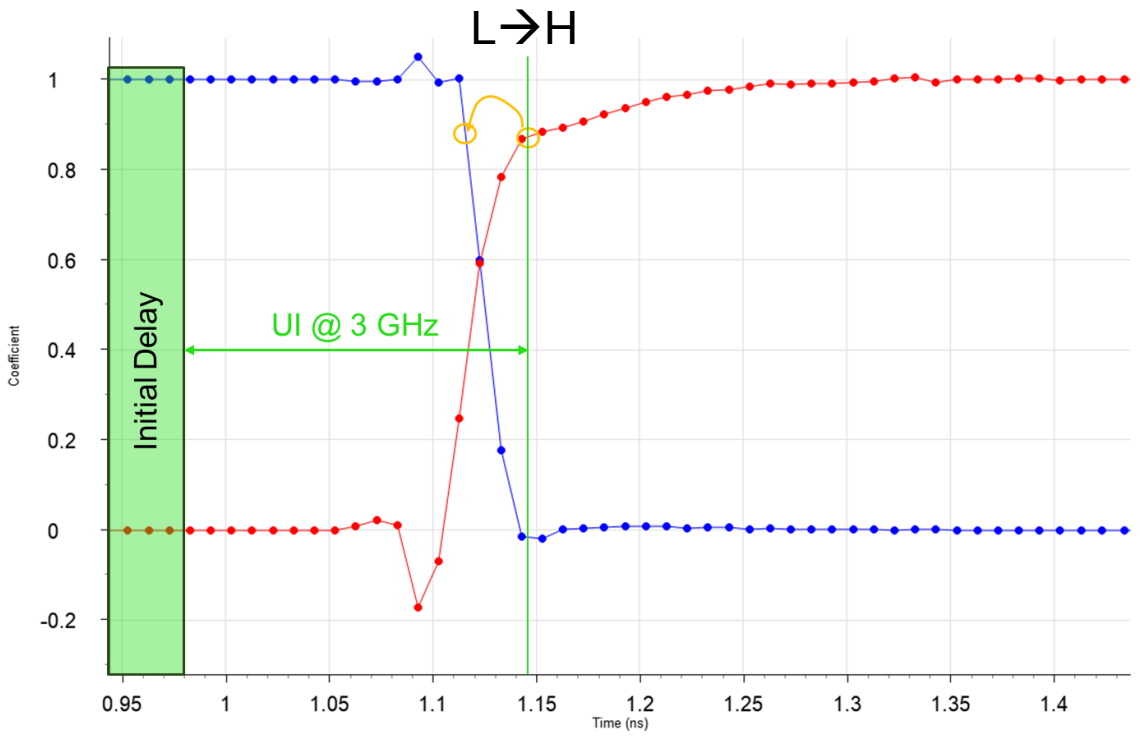
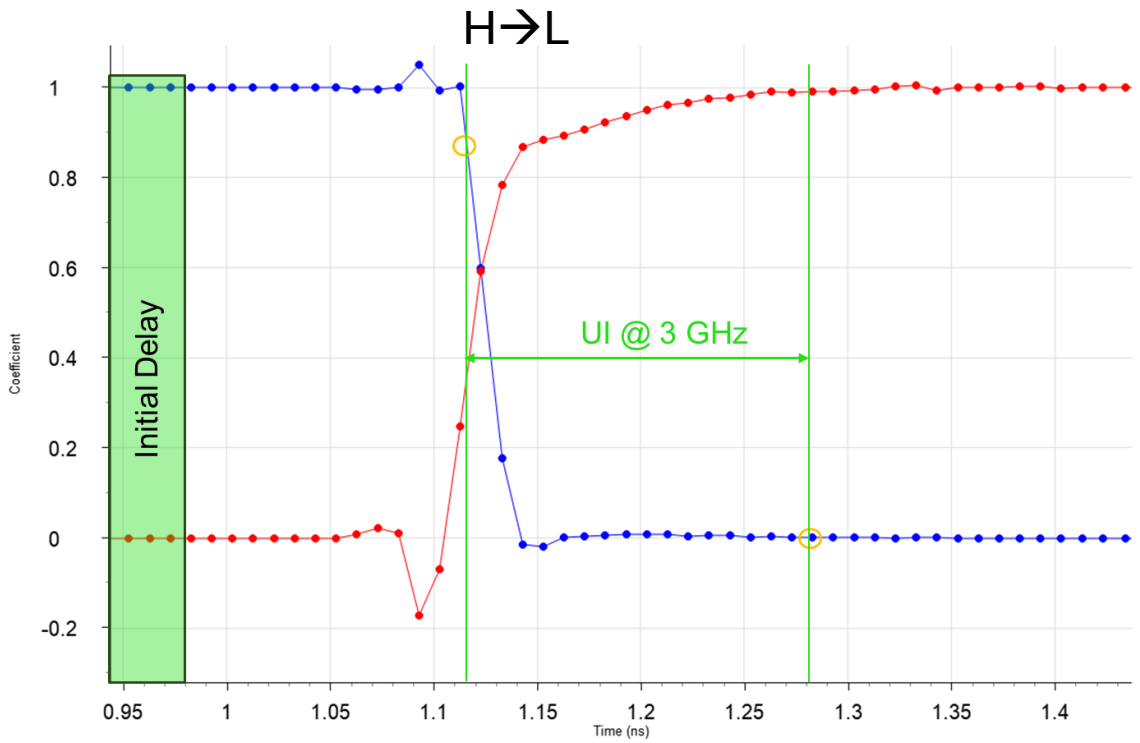
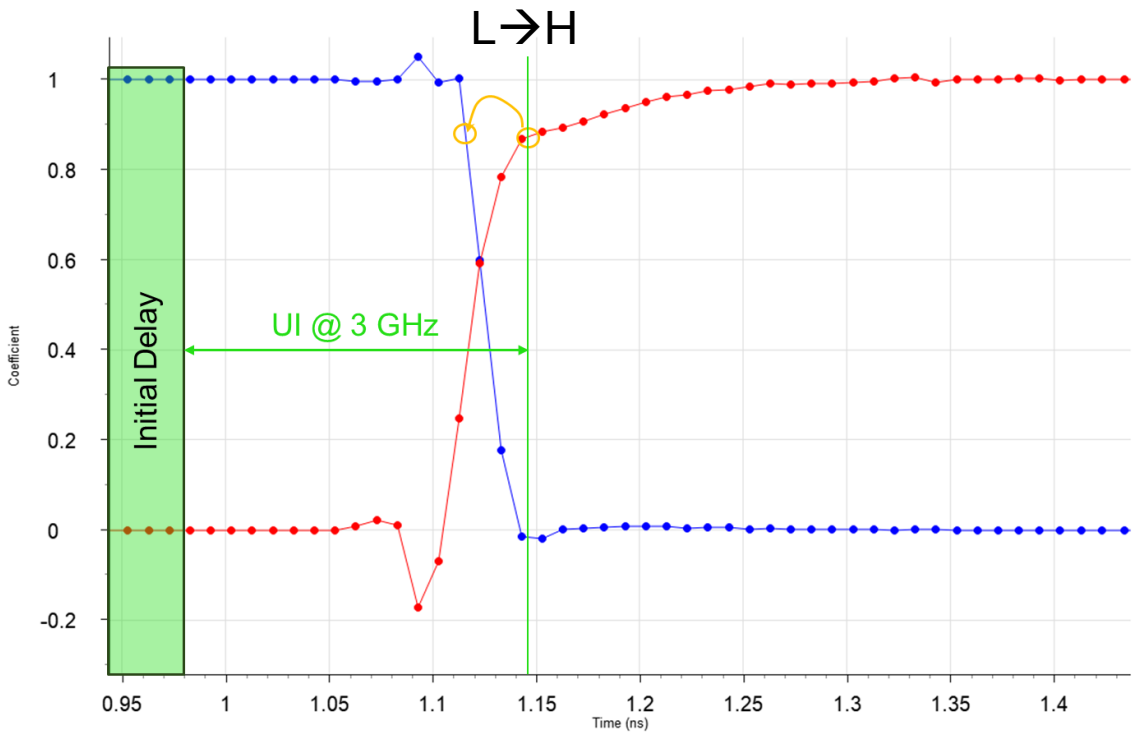


Transition incomplete
→ Determine next starting point from currents



Transition complete
→ Start next UI at original starting point of rising characteristics

Dealing with Overclocking



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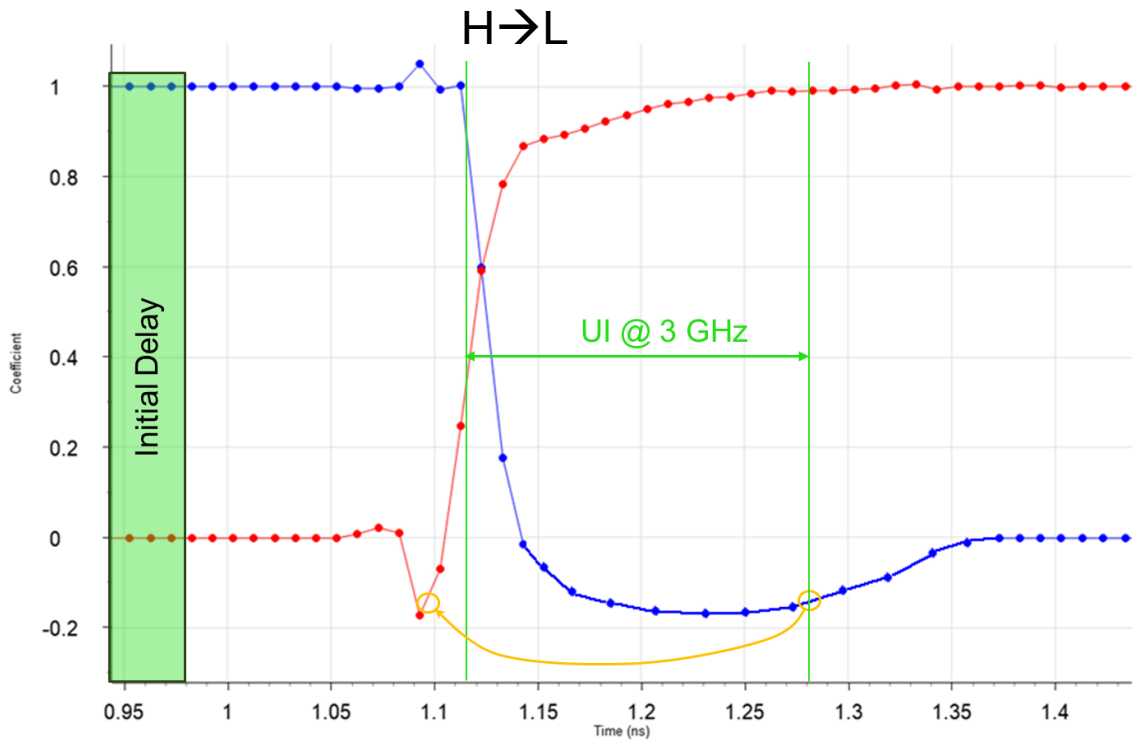

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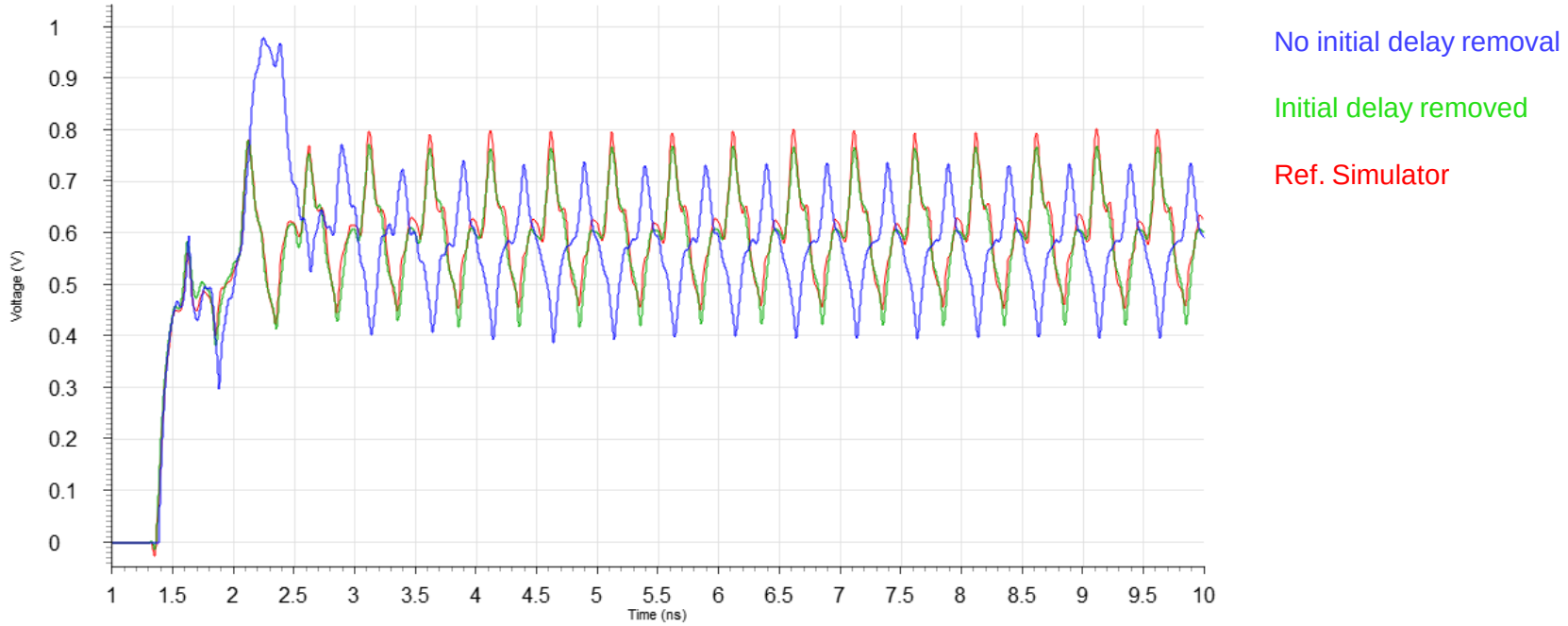
→ Determine next starting point from currents

Some Results

- Initialization
  - In case of overclocking, some initial bits of the time-domain simulation may be required to adjust the timing and position the UI window in the switching characteristic data
  - This depends on the actual model data (e.g. on how quickly a transition is complete)
  - Switching behavior depends on previous state of the transition process



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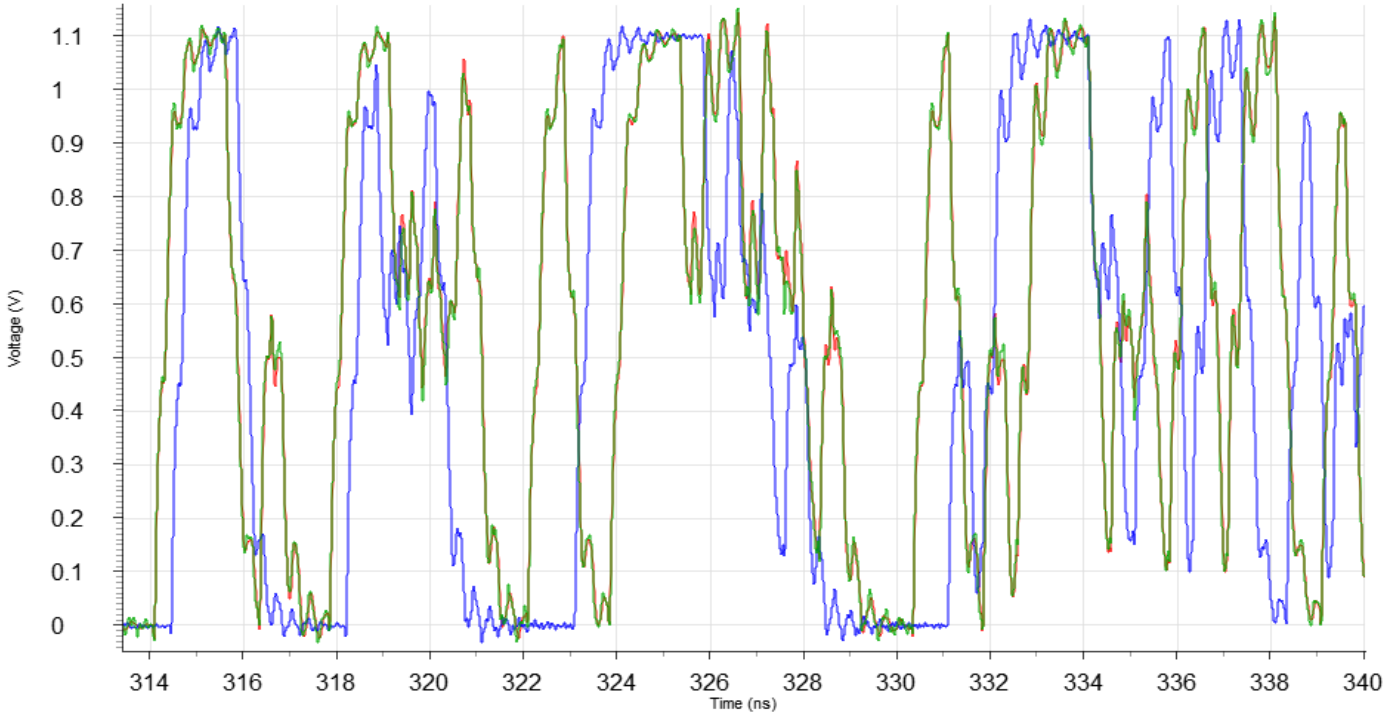

No initial delay removal

Initial delay removed

Ref. Simulator

Some Results

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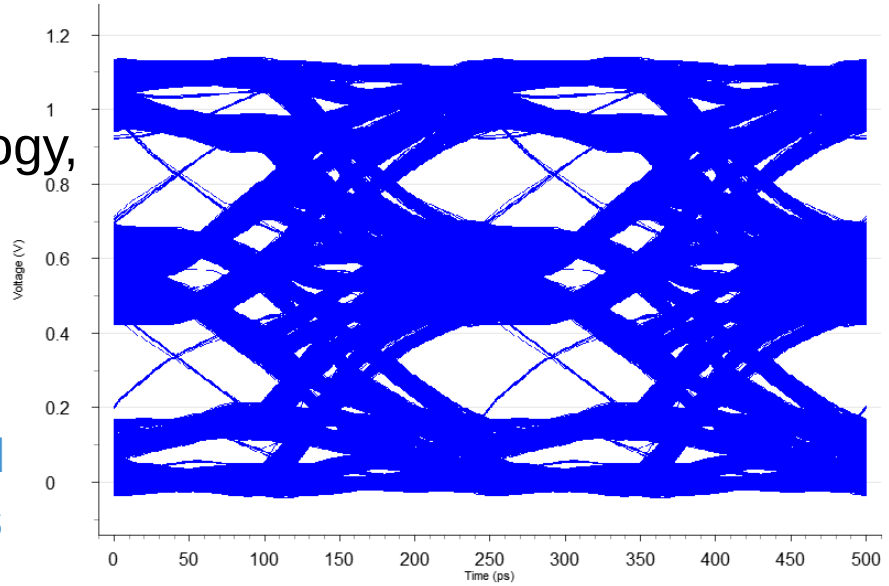
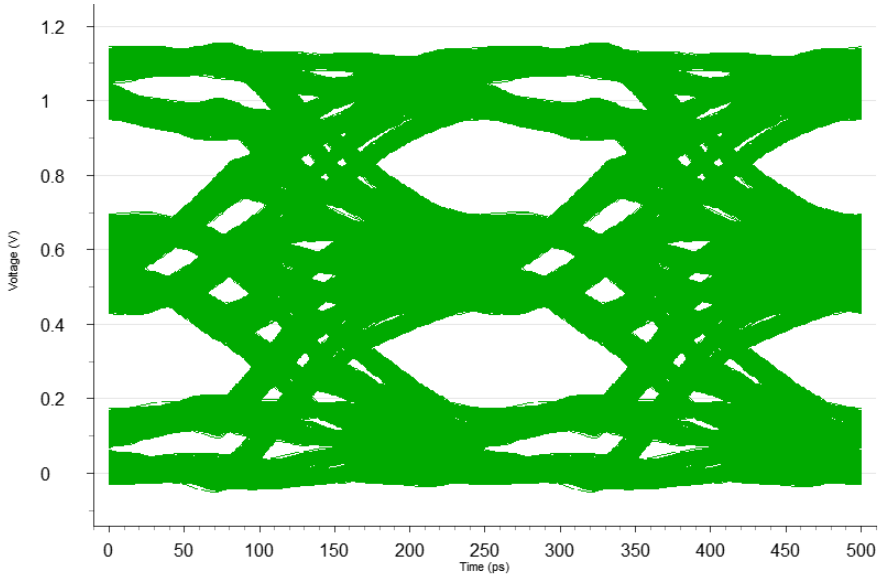
  - Time-domain analysis, **NOT** IBIS AMI





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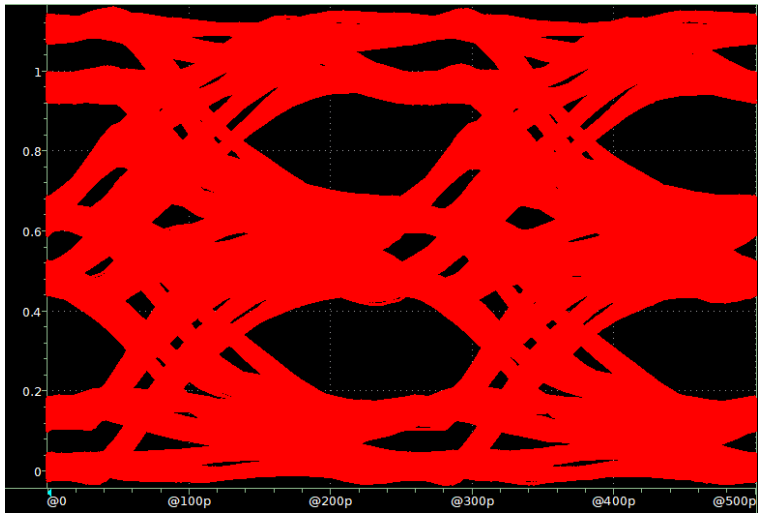

Summary

- Accurate SI Analysis is possible under overclocking conditions
  - For power-aware IBIS models as well
- Initial delays given in IBIS output buffer descriptions need to be treated
  - Too much / *artificial* initial delay cause models to run in overclocking mode, easily
  - Considering timing correlation between switching characteristics and composite currents in power-aware buffer models
    - Hopefully, model makers describe [**`Initial Delay`**] in the model description, properly
    - Otherwise, …
  - EDA Software can improve things and guess the right model behavior, even in unspecified terrain
- However, some model makers could do a better job to be on the safe side…
- Model users rely on correct model data and model interpretation to make correct design decisions

Thanks a lot!
Obrigado!
Danke!

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