Priorities and Alternatives for Touchstone 3.0 Port Mapping

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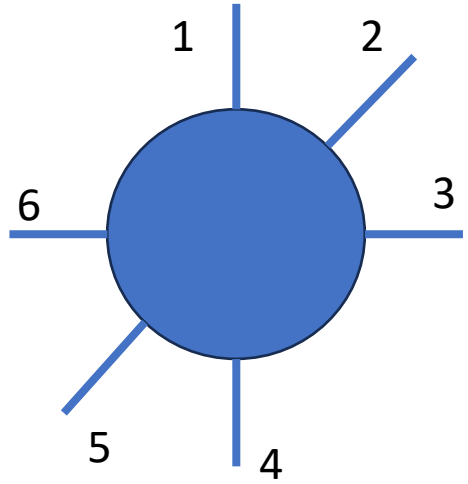
The Problem

- In current Touchstone and Touchstone 2.0, what can I say about the component shown?
  - Interconnect or device?
  - If interconnect, relationship between ports?
  - Can I make inferences from the data?

- Need to know interconnect port arrangement to focus properly on losses vs. crosstalk
  - Is S21 insertion loss? Or is S21 crosstalk?




```
# MHz Y RI R 50
5.00 8.0 9.0 2.0 -1.0 3.0 -2.0 1.0 3.0 1.0 0.1 0.2 -0.2
2.0 -1.0 7.0 7.0 1.8 -2.0 -1.0 -1.0 -0.5 0.5 0.2 -0.1
3.0 -2.0 1.8 -2.0 5.8 6.0 1.2 0.8 0.9 0.7 0.3 -0.5
1.0 3.0 -1.0 -1.0 1.2 0.8 6.3 8.0 2.0 -0.5 1.5 0.6
1.0 0.1 -0.5 0.5 0.9 0.7 2.0 -0.5 4.7 -6.0 -1.0 2.0
0.2 -0.2 0.2 -0.1 0.3 -0.5 1.5 0.6 -1.0 2.0 5.5 -7.0
```

For interconnects, industry wants a structure that establishes expectations for port behavior automatically and in advance of detailed data analysis

Multiple Proposals for Port Mapping (1 of 2)

- The IBIS Interconnect Task Group is considering multiple options to support port-mapping plus other features
  - The two most complete proposals are called here “HL” and “Y” proposals

- Examples and key features of both proposals are shown on the following pages
  - Not all features proposed or under development are shown in the examples

You can find the most recent proposals at
https://ibis.org/interconnect_wip/

Courtesy Walter Katz

Proposed Requirements

1. Define unambiguous connections for simulation
2. Identify Port locations (e.g., xyLayer in PCB)
3. Support automated creation of:
   - Schematic symbols
   - Test probe locations
4. Support generation & verification of:
   - [Interconnect Model]s in .ibs files
   - [EMD Model]s in .emd files
   - [C Comp Model]s in .ibs files
5. Support IEEE 370 data quality features
6. Identify data status (Measured vs. Simulated)
7. Support swathing
8. Support addition of user-defined parameters

Is anything missing?

What is the relative priority of these items?

Courtesy Arpad Muranyi

HL Proposal Syntax Examples (1 of 2)

- Transistor Example

```
[Begin Port Map]
PORT 1 (DESCRIPTION: base) NAME:base
PORT 2 (DESCRIPTION: emitter) NAME:emitter
PORT 3 (DESCRIPTION: collector)  NAME:collector
! ...
CONNECT 1, 2, 3;
[End Port Map]
```

- Simple S4P Example

```
[Begin Port Map]
PORT 1 (DESCRIPTION: Tx_p) NAME:Tx_p SIDE:Tx
PORT 2 (DESCRIPTION: Rx_p) NAME:Rx_p SIDE:Rx
PORT 3 (DESCRIPTION: Tx_n) NAME:Tx_n SIDE:Tx
PORT 4 (DESCRIPTION: Rx_n) NAME:Rx_n SIDE:Rx
! ...
CONNECT 1, 2; 3, 4;
DiffPorts 1, 3; 2, 4;
[End Port Map]
```

Courtesy Arpad Muranyi

HL Proposal Syntax Examples (2 of 2)

Extended Package Example (single-ended, between pin and pad; some connections omitted for space reasons)

```
[Begin Port Map]
PORT 1 +(Pin_I/O_by_PinName, A7, DM_n, S) -(A_gnd) NAME:PinSig_A7_DM_n_A_gnd SIDE:Pin
PORT 2 +(Pad_I/O_by_PinName, A7, DM_n, S) -(A_gnd) NAME:PadSig_A7_DM_n_A_gnd SIDE:Pad
!...
PORT 9 +(Pin_I/O_by_PinName, B3, DQS_c, S) -(A_gnd) NAME:PinSig_B3_DQS_c_A_gnd SIDE:Pin
PORT 10 +(Pad_I/O_by_PinName, B3, DQS_c, S) -(A_gnd) NAME:PadSig_B3_DQS_c_A_gnd SIDE:Pad
PORT 11 +(Pin_I/O_by_PinName, C3, DQS_t, S) -(A_gnd) NAME:PinSig_C3_DQS_t_A_gnd SIDE:Pin
PORT 12 +(Pad_I/O_by_PinName, C3, DQS_t, S) -(A_gnd) NAME:PadSig_C3_DQS_t_A_gnd SIDE:Pad
!...
PORT 20 +(Pad_rail_by_PadName, VSS_DIE-10, VSS, P) -(A_gnd) NAME:PadRail_VSS_DIE-10_VSS_A_gnd SIDE:Pad
CONNECT 1, 2; 9, 10; 11, 12;
DiffPorts 11, 9; 12, 10;
[End Port Map]
```

Courtesy Walter Katz

Y Proposal Syntax Examples & Requirements

- Transistor Example

  [Begin Port Map]
  PORT 1 (Logical Emitter)
  PORT 2 (Logical Base)
  PORT 3 (Logical Collector)
  Left_Side 1
  Right_Side 3
  Bottom_Side 2
  [End Port Map]

- Simple Package Example

  [Begin Port Map]
  PORT 1 (Physical pin.7) (Side Pin) (Net 7) (Logical DQ3pin)
  PORT 2 (Physical pad.7) (Side Pad) (Net 7) (Logical DQ3pad)
  [End Port Map]

Your Input is Needed!

- Is industry looking for increased connectivity features in Touchstone?
  - Are package connections to IBIS, EMD, and IBIS Interconnect directly in the file needed? Or is a “wrapper file” approach acceptable?
  - Should connections to IEEE 370, IEEE 2401 LPB, and/or JEDEC JEP-30 be directly included?
- Is the majority usage model interconnect (as opposed to RF devices)?
- Are naming and functional descriptions per port needed?
- What priority should be given to these new features?
- What has been missed?

Remember that adding features to the specification may add time for finalization and parser development

Backup

Courtesy Arpad Muranyi

HL Proposal Syntax

```
PORT <PortNumber> [+](TermDescriptor) [-(TermDescriptor)] [NAME:<PortName>] [SIDE:<PortSideName>]
  or
PORT <PortNumber> (PortDescriptor) [NAME:<PortName>] [SIDE:<PortSideName>]
```

```
TermDescriptor ::= PinTerm | PinGroupTerm | SigPinTerm | SigPadTerm | SigBufTerm | RailPinTerm | RailPadTerm | RailBufTerm |
                                            PUrefTerm  | PDrefTerm  | PCrefTerm  | GCrefTerm   | EXTrefTerm, S|P
               ::= A_gnd
PortDescriptor ::= DESCRIPTION:<A functional description of the port, perhaps using reserved names>
```

```
PinTerm       ::= PIN:    <RefDes.PinName>, <NetName> | <SignalName>
PinGroupTerm  ::= GROUP:  <GroupName>,       <NetName> | <SignalName>

SigPinTerm    ::= Pin_I/O_by_PinName:     <SignalPinName> | <RefDes.SignalPinName>, <SignalName>
SigPadTerm    ::= Pad_I/O_by_PinName:     <SignalPinName>, <SignalName>
SigBufTerm    ::= Buf_I/O_by_PinName:     <SignalPinName>, <SignalName>

RailPinTerm   ::= Pin_rail_by_PinName:    <RailPinName>    | <RefDes.RailPinName>, <SignalName>
              ::= Pin_rail_by_SignalName: <RailSignalName> | <RefDes.RailSignalName> | <*.RailSignalName>
              ::= Pin_rail_by_BusLabel:   <BusLabelName>   | <RefDes.BusLabelName>   | <*.BusLabelName>

RailPadTerm   ::= Pad_rail_by_PadName:    <PadName>, <SignalName>
              ::= Pad_rail_by_SignalName: <RailSignalName>
              ::= Pad_rail_by_BusLabel:   <BusLabelName>

RailBufTerm   ::= Buf_rail_by_SignalName: <RailSignalName>
              ::= Buf_rail_by_BusLabel:   <BusLabelName>

PUrefTerm     ::= PU_ref_by_PinName:      <SignalPinName>, <SignalName>
PDrefTerm     ::= PD_ref_by_PinName:      <SignalPinName>, <SignalName>
PCrefTerm     ::= PC_ref_by_PinName:      <SignalPinName>, <SignalName>
GCrefTerm     ::= GC_ref_by_PinName:      <SignalPinName>, <SignalName>
EXTrefTerm    ::= Ext_ref_by_PinName:     <SignalPinName>, <SignalName>
```

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HL Proposal Syntax (2)

```
GROUP PORT <PortNumber> [NAME:<GroupName>,] PinList
  or
GROUP_by_Name:<GroupName>, PinList
```

```
PinList ::= <RefDes>.<PinName> | <PinName> | <*.PinName> [, <PinList>]
```