Power Integrity Modeling in IBIS

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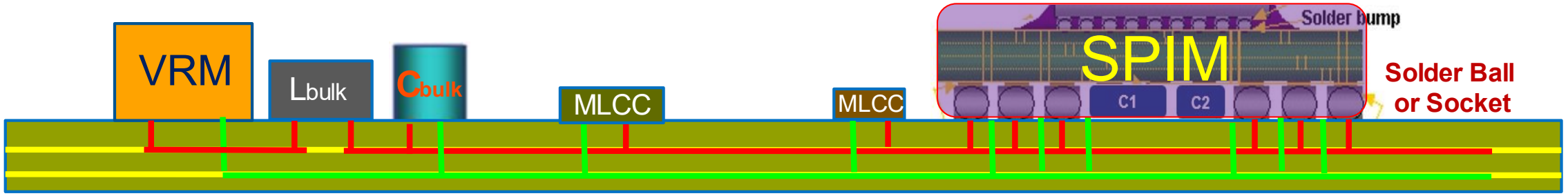
Overview

- Models that are required for a board level power integrity analysis
- PI model has an interconnect model and a silicon load model
- Three kinds of PI analysis, DC, AC and TD (Transient)
- Interconnect model ports have groups of pin, and multiple current loads
- Ground can be Floating or Node 0
- Example of power integrity interconnect models and silicon load models in proposed format

A Board Level Power Delivery Network Consists Of

- Voltage Regulator Module
- Board Level Interconnect
- Package Power Interconnect Models
- Load characterization
  - DC current
  - Current waveform
  - Metrics (Rules)



From BIRD 223.1

A Power Integrity Model consists of Interconnect Model(s) and On-Die Load Model(s)

- Interconnect Model
  - One model for each rail net
  - Touchstone or IBIS-ISS File
  - Pin side terminals, for Power and Ground rails
    - Pin
    - Pin Groups
    - All Pins in Net
  - Silicon side terminals
    - One or more current load
  - Probe definitions
    - Can be associated with dedicated terminals or associated with pins or current loads
- Silicon Load Model
  - DC and AC current source(s)
  - TD PWL waveform current source(s)

Three Kinds of Analysis

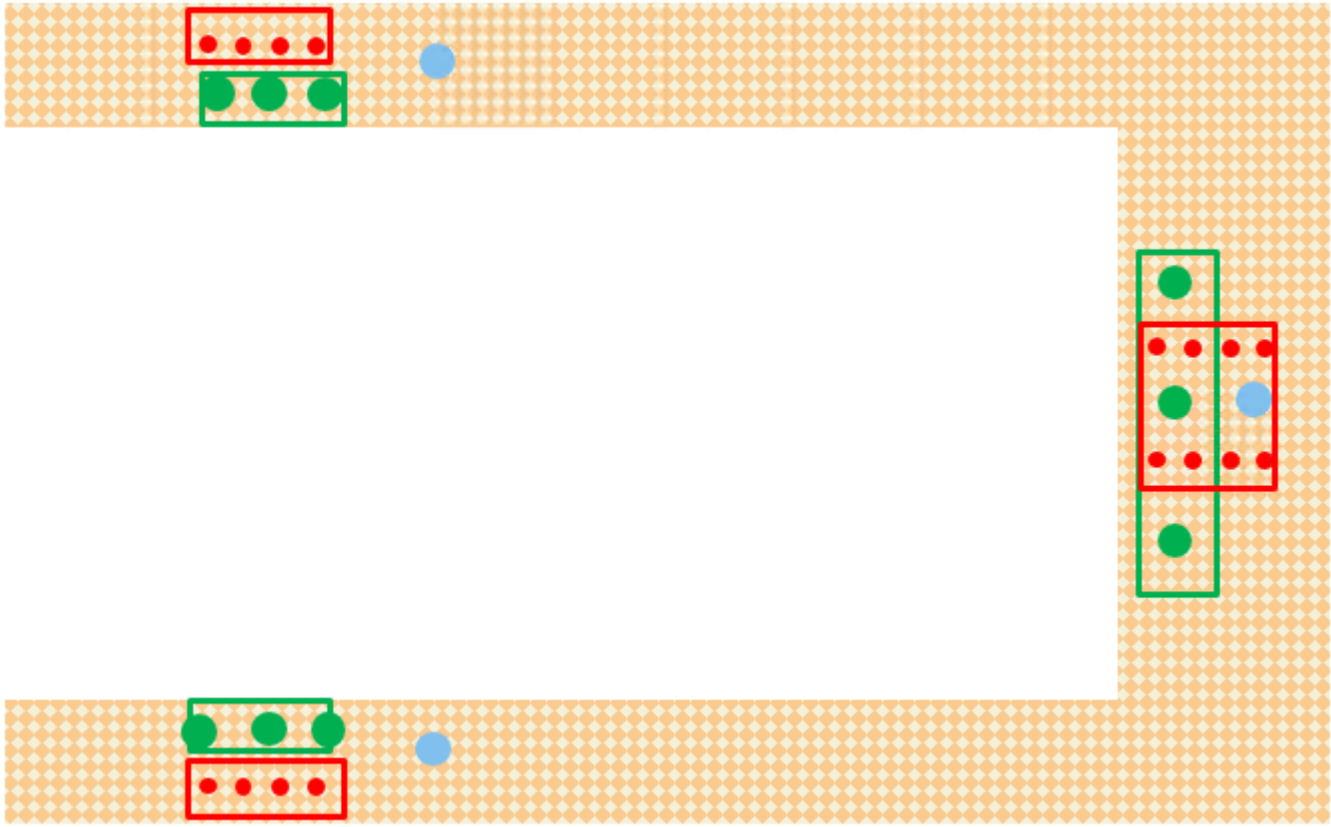
- DC Analysis
  - Currents applied to Load Terminals
  - Voltages measured at Probe locations
    (may include Load Terminals and Pins)
  - Probe definitions include Typ/Min/Max rules
- AC Analysis
  - 1 Amp sinusoidal stimulus distributed among Load Terminals
  - Voltage amplitude is measured at Probe locations
    (may include Load Terminals and Pins)
  - Voltage transfer function is compared to voltage amplitude mask
- TD Analysis
  - PWL current waveform(s) applied to Load Terminals
  - Voltage variations measured at Probe locations
    (may include Load Terminals and Pins)

The Number of Pin and Load Terminals/Ports Determined by the Model Maker is a Tradeoff Between Accuracy and Performance

- Why multiple Load Terminals/Ports
  - Loads are not distributed uniformly on the silicon bump pads
  - Multiple subsystems can be in active or standby state independently
  - Do we need one single TD PWL waveform or one TD PWL waveform for each Load Terminal?

A Modern Package Interconnect for one Rail Net, Size ~2”x2”

- Red Dots are Bumps (Pads)
- Green Dots are Balls (Pins)
- 3 Bump Group Ports (Red Rectangles)
- 3 Ball Group Ports (Green Rectangles)
- 3 Probe Ports (Blue)



- The Balls Connect to the PCB at the Green Dots, Require Pin Numbers to Mate to Board
- The Pads Connect to the Load and the XY coordinates on the Chip are Obfuscated from the User

Ground

- DC analysis
  - Interconnect models are IBIS-ISS resistor networks
  - Model maker can choose to just do DC analysis on Rail interconnect, or do DC analysis on both Rail and Ground interconnect
- AC and TD analysis
  - Interconnect models are IBIS-ISS or Touchstone
  - Model makers can choose A_gnd (SPICE Node 0) as the reference node
  - Model makers can choose a Group of Ground pins as the reference
    - This information is used to mate the interconnect model of the device to the interconnect model of the Board

Pin List Derived from IBIS, EMD File or Local in [PI Model]

[Pin List Import]

file_type	file_reference	component_name
File_IBIS	pp100.ibs	Processor

[End Pin List Import]

[Pin List Import]

file_type	file_reference
File_EMD	board/simm.emd

[End Pin List Import]

[Number of PI Pins] **2000**

[PI Pin List]	signal_name	signal_type	
A1	Vss	GND	
A2	Vdd_1p8	POWER	
A3	Vss	GND	
A4	DQ1		| I/O pin, optional
A5	DQ2		| I/O pin, optional
A6	Vss	GND	
A7	Vdd_1p8	POWER	
A8	Vss	GND	
A9	RFU	NC	
B1	Vss	GND	
B2	Vdd_1p2	POWER	
B3	Vss	GND	
B4	Vdd_1p2	POWER	
B5	Vss	GND	
C1	Vdd_1p2	POWER	
C2	Vss	GND	
C3	Vdd_1p2	POWER	
C4	Vss	GND	

…

[End PI Pin List]

Proposed IBIS Format for Load Current Models, and Rules

[PI Rail] **Vdd_1p8**

[PI Analysis Type] DC
PI_Model_Instance PImodeName2

	V(typ)	V(min)	V(max)
DC_voltage	1.8	1.7	1.9
|	I(typ)	I(min)	I(max)
DC_avg_current	10	9	11

[PI Current Sources]
CurrentSourceName1 0.2
CurrentSourceName2 0.3
CurrentSourceName3 0.5
End PI Current Sources]

[PI Probe] Can be at any terminal

| variable	typ	min	max
IR_drop	100e-3	80e-3	120e-3

[End PI Probe]

[PI Probe] ProbeName or CurrentSourceName or
a pair of pin_name, pin_group, signal_name

| variable	typ	min	max
IR_drop	100e-3	90e-3	110e-3

[End PI Probe]
[End PI Analysis Type]

[PI Analysis Type] AC
PI_Model_Instance PImodeName1
|
[PI Current Sources]
CurrentSourceName1 0.2
CurrentSourceName2 0.3
CurrentSourceName3 0.5
End PI Current Sources]

[PI Probe] Can be at any terminal

Impedance_target	typ	min	max
1.0e4	6.9e-3	NA	NA
1.0e6	6.9e-3	NA	NA
6.5e6	13.0e-3	NA	NA
1.0e7	28.5e-3	NA	NA
2.0e7	28.5e-3	NA	NA

[End PI Probe]

[PI Probe] ProbeName or CurrentSourceName or
a pair of pin_name, pin_group, signal_name

Impedance_target	typ	min	max
1.0e4	6.9e-3	5.0e-3	8.0e-3
1.0e6	6.9e-3	5.0e-3	8.0e-3
6.5e6	13.0e-3	10.0e-3	20.0e-3
1.0e7	28.5e-3	20.0e-3	40.0e-3
2.0e7	28.5e-3	20.0e-3	40.0e-3

[End PI Probe]
[End PI Analysis Type]

[PI Analysis Type] TD
PI_Model_Instance PImodeName1

[PI Current Sources]
CurrentSourceName1 TD_waveform

| time	I(typ)	I(min)	I(max)
0.0	4.0e-3	NA	NA
…			
300.0e-12	0.5e-3	NA	NA

CurrentSourceName2 TD_waveform

| time	I(typ)	I(min)	I(max)
0.0	2.0e-3	NA	NA
…			
300.0e-12	5.0e-3	NA	NA

CurrentSourceName3 TD_waveform

| time	I(typ)	I(min)	I(max)
0.0	1.0e-3	NA	NA
…			
300.0e-12	9.0e-3	NA	NA

[End PI Current Sources]

[PI Probe] Can be at any terminal

| variable	typ	min	max
TD_voltage_variance	150e-3	100e-3	200e-3

[End PI Probe]

[PI Probe] ProbeName or CurrentSourceName or
a pair of pin_name, pin_group, signal_name

| variable	typ	min	max
TD_voltage_variance	150e-3	120e-3	180e-3

[End PI Probe]
[End PI Analysis Type]
[End PI Rail]

[PI Model] Examples (Floating Ground)

```
[PI Model]                PImodelName3
File_TS                   TouchstoneFileName_1p2.s6p
Analysis_type             AC   TD
[PI Pin Groups]
PinGroupName2             (B2 B4)
PinGroupName3             (B1 B3 B5)
PinGroupName4             (C1 C3)
PinGroupName5             (B5 C2 C4)
[End PI Pin Groups]
Number_of_ports = 6
1     PI_Pin              pin_group     PinGroupName2          pin_group     PinGroupName3
2     PI_Pin              pin_group     PinGroupName4          pin_group     PinGroupName5
3     PI_Current          source        CurrentSourceName1
4     PI_Current          source        CurrentSourceName2
5     PI_Probe            probe         ProbeName1
6     PI_Probe            probe         ProbeName2
[End PI Model]
```

```
[PI Model]                PImodelName4
File_IBIS-ISS             SPICEfileName_1p2.ckt      SubcktName
Analysis_type             DC
[PI Pin Groups]
PinGroupName2             (B2 B4)
[End PI Pin Groups]
Number_of_terminals = 12
1     PI_Pin              pin_group     PinGroupName2
2     PI_Pin              signal_name   Vss
3     PI_Pin              pin_name      C1
4     PI_Pin              pin_name      C3
5     PI_Current          source_p      CurrentSourceName1
6     PI_Current          source_n      CurrentSourceName1
7     PI_Current          source_p      CurrentSourceName2
8     PI_Current          source_n      CurrentSourceName2
9     PI_Probe            probe_p       ProbeName1
10    PI_Probe            probe_n       ProbeName1
11    PI_Probe            probe_p       ProbeName2
12    PI_Probe            probe_n       ProbeName2
[End PI Model]
```

[PI Model] Examples (Node 0 Ground)

[PI Model] **PImodelName3**
File_TS TouchstoneFileName_1p2.s6p
Analysis_type AC TD
[PI Pin Groups]
PinGroupName2 (B2 B4)
PinGroupName4 (C1 C3)
[End PI Pin Groups]
Number_of_ports = 6

1	PI_Pin	pin_group	PinGroupName2
2	PI_Pin	pin_group	PinGroupName4
3	PI_Current	source	CurrentSourceName1
4	PI_Current	source	CurrentSourceName2
5	PI_Probe	probe	ProbeName1
6	PI_Probe	probe	ProbeName2

[End PI Model]

[PI Model] **PImodelName4**
File_IBIS-ISS SPICEfileName_1p2.ckt SubcktName
Analysis_type DC
[PI Pin Groups]
PinGroupName2 (B2 B4)
[End PI Pin Groups]
Number_of_terminals = 7

1	PI_Pin	pin_group	PinGroupName2
2	PI_Pin	pin_name	C1
3	PI_Pin	pin_name	C3
4	PI_Current	source_p	CurrentSourceName1
5	PI_Current	source_p	CurrentSourceName2
6	PI_Probe	probe_p	ProbeName1
7	PI_Probe	probe_p	ProbeName2

[End PI Model]

[PI Model] - Touchstone Syntax

<Port_number> <Port_type> <+Port_type_qualifier> <+Qualifier_entry> <-Port_type_qualifier> <-Qualifier_entry>

```
[PI Model]          PImodelName
File_TS             TouchstoneFileName_1p8.s6p
Analysis_type       AC   TD
Number_of_ports = 6
1     PI_Pin        pin_name      POWERpinName
                    pin_group     POWERpinGroupName
                    signal_name   POWERpinSignalName
                    pin_name      GNDpinName
                    pin_group     GNDpinGroupName
                    signal_name   GNDpinSignalName
                    A_gnd
…
3     PI_Current    source        CurrentSourceName1
…
6     PI_Probe      probe         ProbeName1
…
[End PI Model]
```

```
[PI Model]          PImodelName
File_TS             TouchstoneFileName_1p8.s6p
Analysis_type       AC   TD
Number_of_ports = 6
1     PI_Pin        pin_name      POWERpinName
                    pin_group     POWERpinGroupName
                    signal_name   POWERpinSignalName
…
3     PI_Current    source        CurrentSourceName2
…
6     PI_Probe      probe         ProbeName2
…
0     PI_Ref        pin_name      GNDpinName
                    pin_group     GNDpinGroupName
                    signal_name   GNDpinSignalName
                    A_gnd
[End PI Model]
```

- **Options listed in the red and blue boxes may be mixed in any combination for the PI_Pin port type (2N syntax)**
- **If -Port_type_qualifier and -Qualifier_entry are not provided for the negative port terminals, a PI_Ref line may be used to define what they are connected to (N+1 syntax)**
- **If a PI_Ref line is not provided either, the negative port terminals are connected to A_gnd**
- **The "+" and "-" terminals of sources and probes are always connected to the "+" and "-" terminals of their corresponding Touchstone file port**

[PI Model] - IBIS-ISS syntax

<Terminal_number> <Terminal_type> <+Terminal_type_qualifier> <+Qualifier_entry> <-Terminal_type_qualifier> <-Qualifier_entry>

```
[PI Model]              PImodelName
File_IBIS-ISS           SPICEfileName_1p8.ckt        SubcktName
Analysis_type           DC  AC  TD
Number_of_ports = 16
1     PI_Pin            pin_name        POWERpinName
                        pin_group       POWERpinGroupName
                        signal_name     POWERpinSignalName
…
3     PI_Pin            pin_name        GNDpinName
                        pin_group       GNDpinGroupName
                        signal_name     GNDpinSignalName
                        A_gnd
…
7     PI_Current        source_p        CurrentSourceName1
8     PI_Current        source_n        CurrentSourceName1
…
15    PI_Probe          probe_p         ProbeName1
16    PI_Probe          probe_n         ProbeName1
[End PI Model]
```

```
[PI Model]              PImodelName
File_IBIS-ISS           SPICEfileName_1p8.ckt        SubcktName
Analysis_type           DC  AC  TD
Number_of_ports = 15
1     PI_Pin            pin_name        POWERpinName
                        pin_group       POWERpinGroupName
                        signal_name     POWERpinSignalName
…
3     PI_Pin            pin_name        GNDpinName
                        pin_group       GNDpinGroupName
                        signal_name     GNDpinSignalName
                        A_gnd
…
7     PI_Current        source_p        CurrentSourceName2
…
15    PI_Probe          probe_p         ProbeName2
[End PI Model]
```

```
pin_name        GNDpinName
pin_group       GNDpinGroupName
signal_name     GNDpinSignalName
A_gnd
```

```
pin_name        GNDpinName
pin_group       GNDpinGroupName
signal_name     GNDpinSignalName
A_gnd
```

- **If the negative terminal of a source or probe does not have a dedicated subcircuit terminal, a -Terminal_type_qualifier and -Qualifier_entry must be provided for them to define what they are connected to. Note: -Terminal_type_qualifier and -Qualifier_entry define how to connect the "-" terminals of sources and probes in the context of File_IBIS-ISS, as opposed to defining how to connect the "-" terminals of Touchstone ports in the context of File_TS.**