Micron’s IBIS Model Quality Process

Asian IBIS Summit
Shanghai, China
November 11, 2008

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Overview

• Micron builds in quality checks into each step of the model creation process
  ‣ Spice netlist creation
  ‣ IBIS creation process

• Quality Report documentation for customers

• Conclusions
Spice netlist creation

• Multiple pre-driver stages are included - critical timing paths unmodified

• Standard Parasitic Format (SPF) netlists are created for circuits with completed layouts

• SPF includes two flavors
  ‣ C only – Capacitance of all layout structures included
  ‣ RC – Resistance and Capacitance included
  ‣ RC is more accurate but creates unreasonably large netlists
  ‣ C only with additional PRC elements on critical nets can approach accuracy of RC netlist but be much smaller
Spice Netlist: SPF Format Effect on Vox

In this example, PRC elements were needed to properly model the effect of long, imbalanced metal lines between the pre-driver logic and pre-driver stages.

Quality ☑️: Correct Vox level
Determining C_comp min/max

\[ C_{\text{model\_min}} = C_{\text{package}} + C_{\text{comp\_min}} \]

\[ C_{\text{model\_max}} = C_{\text{package}} + C_{\text{comp\_max}} \]

Quality √: Correct C_package and C_comp
Correlating I-V curves to Measurements

- Must match exact Process/Voltage/Temp conditions between Spice simulation and Measurement
- Process model adjustment example
  - Process corners set by parameter range: -1=Slow, 0=Typical, 1=Fast
  - IDSN model corners (uA/um) (for specific Vds and Vgs voltage setting)
    - Slow: 359.0 Typical: 399.8 Fast: 450.9
    - Silicon Measurement: 397.3, Adjusted 6.1% towards Slow (-0.061)
  - IDSP model corners (uA/um)
    - Slow: 173.1 Typical: 203.7 Fast: 242.1
    - Silicon Measurement: 194.1, Adjusted 31.5% towards Slow (-0.315)
Correlating I-V curves to Measurements

- Model = yellow, Measurement = red

Before PVT Adjustment

After PVT Adjustment

Quality ✓: I-V curves match measurements
Model Quality

• Model Creation Checklists
  ‣ Spice model development
    ✓: Transistor model libraries setup and correlated to speed grades
    ✓: Correct power supply decoupling included in netlists
    ✓: Variable capacitance added to PAD node for proper $C_{comp}$ variation
    ✓: Clamp diode currents adjusted through bulk node resistance
    ✓: All control signal combinations function properly
Model Quality

• Model Creation Checklists
  ‣ IBIS model development
    ✓: Run IBISCHK – explain any warnings
    ✓: Component names and Pin lists agree with the datasheet
    ✓: Input model parameters match the datasheet
    ✓: I/O model parameters match the datasheet
    ✓: V-t curves time correlated and on/off time relationships valid
    ✓: Combined Submodel curves show proper ODT voltage midpoint termination and resistance
Quality Reports

• IBIS Open Forum – IBIS Quality Task Group
  ‣ Released the IBIS Quality Specification, Rev 1.0, 3/31/04
  ‣ Currently working on an updated release

• Micron follows the IQ Spec, but releases a detailed report with each model
  ‣ Compares model to specification data
  ‣ Compares model to measurement data
  ‣ Compares IBIS model to HSPICE model
Quality Reports - Introduction

IBIS/HSPICE Model Quality Report

Design ID: T35M
Description: 128Mb Mobile DDR SDRAM
Marketing device name(s): MT46H8M16LFBF, MT46H4M32LFB5, MT46H8M16LFT35M, MT46H4M32LFT35M
Valid Speed Grades: -75 (266), -6 (333), -54 (370), -5 (400)
Zip File Name: t35m_ibis.zip, t35m_it_ibis.zip
IBIS File name: t35m.ibs, t35m_it.ibs  File rev: 2.0, 2.0
HSPICE File name: t35m_hspice.zip  File rev: 2.0
EBD file name (if applicable):  File rev:
Die Rev: K
Date: October 8, 2008
Datasheet Link:
http://download.micron.com/pdf/datasheets/dram/mobile/128mb_mobile_ddr_sdram_t35m.pdf

E-mail at modelsupport@micron.com for questions regarding Quality Report

Device Parameters

VDDQ – Slow: 1.70  Typical: 1.80  Fast: 1.95
VDD – Slow: 1.70  Typical: 1.80  Fast: 1.95
Junction Temperature (Commercial) - Slow: 85  Typical: 40  Fast: 0
Junction Temperature (Industrial) - Slow: 100  Typical: 40  Fast: -40
VDDQ/VSSQ Decoupling Capacitance: 2.76nF
  Included in HSPICE DQ/DQS models? yes  Amount per DQ/DQS model: 76.66pF
VDDQ/VSSQ Decoupling Capacitance Series Resistance: 1 ohm
Quality Reports – IQ Summary

• IBIS Quality Summary included based on IQ 1.0 specification
• Report will detail IQ 1.1 spec once released
• IBIS model does not include full IQ Summary, but instead states:
  | IQ SUMMARY Overall Quality of component and models Level 2b
  | See Micron IBIS Model Quality Report for full IQ SUMMARY
Quality Reports – IOH/IOL vs. Spec
Quality Reports – C_comp, ODT & Slew Rates vs. Specification

### C_comp

<table>
<thead>
<tr>
<th>DQ</th>
<th>IBIS</th>
<th>Datasheet (DDR3-1600)</th>
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<td>max</td>
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<td>C_total</td>
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<td>1.5pF</td>
<td>2.3pF</td>
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<td>INPUT</td>
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<td>C_comp</td>
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### ODT

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<th></th>
<th>TYP</th>
<th>MIN</th>
<th>MAX</th>
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<tbody>
<tr>
<td>Vinl (V)</td>
<td>0.575</td>
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<td>0.6125</td>
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<tr>
<td>Vinh(V)</td>
<td>0.925</td>
<td>0.8875</td>
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<td>linl (A)</td>
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<td>linh (A)</td>
<td>0.007425</td>
<td>0.00615</td>
<td>0.00789</td>
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<tr>
<td>Rtt (Model)</td>
<td>23.77</td>
<td>22.12</td>
<td>27.03</td>
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<td>Rtt (datasheet-in units of ZQ/12)</td>
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<td>Rtt (datasheet)</td>
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### Slew Rates

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<tr>
<th>Model</th>
<th>Slew Rate (V/ns)</th>
<th>Simulation</th>
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Quality Reports – C_comp & IOH/IOL vs. Measurement

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<th>IBIS</th>
<th>Measured</th>
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C_comp

IOH/IOL
Quality Reports – IBIS vs. HSPICE

Test load

- T-line: Z0 = 50 ohms, Td = 0.5 ns

Diagram showing waveforms for various conditions.
Conclusions

• Model users demand quality models

• IBIS Quality Committee work is essential for standardizing quality levels and methods

• IBIS Quality checklists work to maintain quality standards

• Quality Reports go above and beyond checklists to document thorough model checking

• Demand Quality models from vendors!
  ‣ Show them examples of quality models.