Noise Countermeasure Design Technology for Signal and Power Integrity

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1. Background

Speed Up of Operating Frequency

- Serial Transmission
  - FibreChannel
- Parallel Transmission
  - DDR
  - AGP
  - SDRAM
- PCI-e
  - PCI-e Gen2
  - XFI/10Gb

Data Rate [Gbps/ch]

- 350nm
- 250nm
- 180nm
- 130nm
- 90nm
- 65nm

Process

YEAR

1995  2000  2005  2010
1. Background

Lowering of Supply Voltage

Supply voltage: Lowering → Allowable power noise: Smaller
2. Tasks

Emerging of Noise Problem

1. Signal Integrity (SI)
   (1) Reflection noise, Crosstalk noise
   (2) Skin effect, Dielectric loss
   (3) ISI: Inter Symbol Interference

2. Power Integrity (PI, power noise)
   (1) Simultaneous switching noise
   (2) Voltage and ground bounce noise
   (3) Noise caused by return current

3. EMC
   (1) EMI
   (2) ESD

4. Composite Noise
   Complex noise problems composed of SI, PI and EMI/ESD etc..
   Ex. Deterioration of cell phone antenna sensitivity
3. Countermeasures

Simulation based Design

Signal Integrity

Power Integrity

EMC(EMI, ESD)

Full automatic verification
Advice for design condition
Multi-Gbps analysis

Middle scale
Large scale

EMI
ESD
Return Current

LSI, PCB Unified Analysis

Technical Computing
- Large Scale Analysis
- High Speed Analysis

1995
2000
2005
NOW

1995 2000 2005

NOW

LSI core noise
IO SSO noise

Driver LSI
PKG

PCB

mutual Interference

EMI from Signal Pattern

Receiver LSI

EMI from V/G Layer

PCB G Noise

LSI Power Noise Analysis

LSI, PCB Unified Analysis

Technical Computing
- Large Scale Analysis
- high Speed Analysis

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4. LSI, PCB Unified Noise Analysis

**Occurring principle of Power noise**

- Power noise: \( \Delta V = -Z(f) \times \Delta I_p \)
- V/G Impedance: \( Z(f) \leq \Delta V_{\text{max}} / \Delta I_p = \text{Allowable Impedance} \)

**Equivalent Circuit of LSI, PCB and voltage supply**

- Supply Current: \( I_p(t) \)
- Voltage Supply
- LSI
- Decoupling Capacitor
- V/G Plane
4. LSI, PCB Unified Noise Analysis

Tasks

High accuracy power noise analysis

V/G impedance

Allowable impedance

Allowable impedance decreasing caused by frequency increasing and supply voltage decreasing

Suppressing V/G impedance under the allowable impedance become more difficult

High accuracy power noise analysis method is required
4. LSI,PCB Unified Noise Analysis

Tasks

More Detailed Equivalent Circuit of LSI,PCB and voltage supply
4. LSI, PCB Unified Noise Analysis

Tasks

- LSI, PCB Unified Noise Analysis

- Using LSI model
- Using PCB model
- Using LSI and PCB model

②, ③ models have large calculation error

LSI, PCB unified model is essential for high accuracy
4. LSI, PCB Unified Noise Analysis

Tasks

- Delay variation of signal and clock
- Split clock waveform

**SI and PI Problem should be solved simultaneously**

- Power noise
- Signal waveform
- Delay variation

Waveform split by power noise
4. LSI, PCB Unified Noise Analysis

System configuration

LSI model Generation → Floor Planner → Layout CAD → Data Converter

Other Layout CAD

Device Characteristic Definition

Purchased LSI Model
Voltage Supply Device Condenser

Intra-LSI Model
PCB CAD Data

Power Noise Analysis System

LSI, PCB Unified Model

Circuit Simulator

V/G Impedance

Power Noise Waveform

EMI Solver

Calculated EMI
4. LSI, PCB Unified Noise Analysis

**LSI, PCB Unified model**

- **IO cell:** SPICE model
  - Behavior model
- **LSI core:**
  - Distributed current Source
- **Intra-LSI V/G:**
  - Lattice of LCR SPICE model
- **V/G Pin:**
  - LCR model
- **Package:**
  - LCR model

**IBIS models not suitable for power noise analysis**

- **Purchased LSI:**
  - IBIS model (IO Model, PKG)
- **Board V/G:**
  - LCR Mesh model
- **Wiring/via:**
  - LCR ladder model
- **Bypass condenser:**
  - (C, ESL, ESR)
  - Draw out wiring

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High Speed Transmission Waveform Simulation with Power noise

Power Noise Waveforms calculated by LSI, PCB Unified Analysis

Added to V/G pins of IO models

Eye pattern diagram

IBIS models not suitable for such a method

Transmission waveform simulator

IO model
- SPICE
- Behavior

W-element model

This method significantly shortens the calculation time comparing to the full LSI, PCB Unified Analysis with the comparable accuracy.
4. LSI, PCB Unified Noise Analysis

Two typical operating flows

LSI design stage (Pre-simulation flow)
- Optimizing noise countermeasure design of LSI and PCB
  - LSI IO selection, Pin Layout, decoupling capacitor, PKG selection
  - PCB design conditions (layer configuration, topology, decoupling Capacitor)

LSI, PCB design verification stage (Post-simulation flow)
- Noise verification of LSI and PCB taking account of mutual interference

- Avoiding LSI remake, Reducing PCB trial production
- Reducing number of parts
- Shortening design and evaluation term
4. LSI, PCB Unified Noise Analysis

**Pre-Simulation flow**

- **Rough parts definition (Minimizing input information)**
- **FloorPlanner**
  - Board Spec.
  - Device Char.
  - LSI Spec.
  - LSI Model

- **Parts layout study**
- **Wiring strategy study**
- **V/G design study**

**Flow Diagram**

- **Transmission line analysis**
- **Signal Integrity**
- **Power Integrity**
- **EMC**
- **Power noise analysis**
- **EMI analysis**

- **LSI specification**
- **PCB design constraints**
4. LSI, PCB Unified Noise Analysis

Evaluation results of analysis accuracy

Accuracy of V/G noise analysis by evaluation LSI and PCB
4. LSI, PCB Unified Noise Analysis

Evaluation results of analysis accuracy

Accuracy of V/G noise analysis by evaluation LSI and PCB

- Rise → I/O (27 Sig.) → Fall
- Simultaneously Switching
- 20MHz

- Black: measured
- Red: simulated

- VDE-VREF
- VDD-VREF
- VSS-VREF

- SSO
5. Application Results

Example of V/G Impedance Analysis

V/G mesh model

Results of V/G Impedance Analysis

Capacitors around LSI

Capacitors on backside of LSI

0.1μF (2012)  
0.1μF (1005)  
1μF  
10μF  
470μF
### V/G Impedance Calculation Results of Various PCBs

<table>
<thead>
<tr>
<th>No.</th>
<th>PCB size (cm²)</th>
<th>Number of PCB layer</th>
<th>Calculation time (HH:MM:SS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>106</td>
<td>6</td>
<td>0:01:24</td>
</tr>
<tr>
<td>2</td>
<td>43</td>
<td>6</td>
<td>0:26:19</td>
</tr>
<tr>
<td>3</td>
<td>1036</td>
<td>12</td>
<td>0:20:03</td>
</tr>
<tr>
<td>4</td>
<td>1398</td>
<td>12</td>
<td>3:08:13</td>
</tr>
<tr>
<td>5</td>
<td>1061</td>
<td>22</td>
<td>7:57:53</td>
</tr>
<tr>
<td>6</td>
<td>2184</td>
<td>22</td>
<td>25:07:02</td>
</tr>
</tbody>
</table>
5. Application Results

V/G Impedance Analysis Using Floor Planner

Analysis Model

【Specification of Analyzed PCB】

<table>
<thead>
<tr>
<th>PCB size (㎠)</th>
<th>Number of PCB layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>10</td>
</tr>
</tbody>
</table>

【Using Floor Planner CAD Data】

【Using Layout CAD Data】
5. Application Results

V/ G Impedance Analysis Using Floor Planner

Analysis Result

Calculation Time

<table>
<thead>
<tr>
<th>CAD Data</th>
<th>Model Size</th>
<th>Calculation Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floor Planner</td>
<td>2MB</td>
<td>0:01:37</td>
</tr>
<tr>
<td>Layout CAD</td>
<td>50MB</td>
<td>4:52:00</td>
</tr>
</tbody>
</table>

x180 faster

Power noise countermeasure from floor planning stage enables us to easily determine Power design constraint.

(Decoupling capacitors, V/G layer construction, V/G layer partition)
5. Application Results

Example of LSI, PCB Unified Noise Analysis

System configuration

Optimizing noise countermeasure design by LSI, PCB unified noise analysis

Developed LSI

DDR-SDRAM

66MHz/32bit Local Bus

266MHz/64bit
5. Application Results

Example of LSI, PCB Unified Noise Analysis

V/G impedance analysis (without decoupling capacitors)

- Allowable impedance @1.8V (worst condition)
- 160 kHz
- DDR Operating frequency (266MHz)
5. Application Results

Example of LSI, PCB Unified Noise Analysis

V/G impedance analysis (with decoupling capacitors)

Allowable impedance @1.8V (worst condition)

Suppress impedance under allowable impedance

DDR Operating frequency (266MHz)
5. Application Results

Example of LSI, PCB Unified Noise Analysis

Verification of DDR data delay variation caused by V/G noise

Delay variation is within allowable value
6. Conclusion

- Fujitsu’s LSI, PCB Unified Noise Analysis System were introduced and the effectiveness of the system were explained.

- Further developments of the noise countermeasure design system to overcome the rapid advances of technology are scheduled.
7. Future Tasks

- The LSI, PCB Unified Noise Analysis Technology has been established as explained today. But, it is difficult to obtain the various LSI models available for power noise analysis (DDR, FPGA, ASIC, ASSP • • •).

- Sufficient supply of LSI power noise models are required.

- It is one of the most desirable solutions for this problem that the standard IBIS models available for power noise analysis are widely supplied by LSI vendors.

- We hope IBIS Forum and JEITA will promote to establish the standard IBIS model for power noise analysis and spread it widely as a future task.
THE POSSIBILITIES ARE INFINITE