System-level Serial Link Analysis using IBIS-AMI Models

Todd Westerhoff, SiSoft
twesterh@sisoft.com

Asian IBIS Summit
Tokyo, Japan
November 14, 2008
Agenda

- Serial Link Analysis
- IBIS Algorithmic Modeling Interface (IBIS-AMI)
- Network Characterization
- Statistical Analysis
- Time-Domain Analysis
- IBIS-AMI Simulation Performance
- Correlation
- Summary
SerDes Analysis Requirements

• User requirements
  – Multi-million bit simulations
  – Model specific SerDes IP
    • Equalization
    • Clock recovery
  – Analyze channel & SerDes IP tradeoffs
  – Support lab correlation (eye height/width, BER, etc.)

• SerDes vendor requirements
  – Protect SerDes IP
  – Single model supported in multiple EDA tools
Traditional SerDes Simulator Flow

Network Characterization

Link Analysis

Pulse Response

TX EQ  RX EQ

SerDes Simulator

Eye Statistics

Pulse Response

Pulse Response
Traditional SerDes Challenges

• SerDes vendor tools don’t work together
  – Simulating cross-vendor links is difficult or impossible
• Open-source tools lack IP vendor models

Observation

• Most SerDes tools take S-parameter or pulse response data, then use signal-processing & statistical techniques to predict behavior
• A standardized SerDes analysis flow and model format would address both user & SerDes vendor issues
IBIS Algorithmic Modeling Interface (IBIS-AMI)

- Part of the approved IBIS 5.0 specification
- Divides SerDes simulation into two parts
  - Network characterization
    - Determines impulse response for unequalized analog network
  - Communications analysis
    - Models TX/RX equalization and clock recovery behavior
    - SerDes IP models are provided as executable code linked into the simulator at run time
- Standard mechanism for declaring model-specific parameters
IBIS-AMI Models

An IBIS-AMI model has two parts:

**Analog Model**
- Used to model behavior of the unequalized analog network (Network Characterization)
- TX: output impedance & parasitics
- RX: receiver input termination network & parasitics

**Algorithmic Model**
- Used to perform end to end link analysis including equalization and clock recovery behavior
- Models supplied as loadable object code
- Models can operate at two different levels:
  - INIT: impulse response processing
  - GETWAVE: time-domain waveform processing
Model-Specific Parameters

**IBIS File**

```plaintext
[Algorithmic Model]
Executable Windows SiSoft_AMI_Tx.dll Sample_AMI_Tx.ar
Executable Solaris SiSoft_AMI_Tx.solaris.so Sample_AMI_Tx.ar
Executive Linux SiSoft_AMI_Tx.linux.so Sample_AMI_Tx.ar
[End Algorithmic Model]
[Temperature Range] 25 100 C
[Voltage Range] 1.0 0.95 1.05

[Pulldown]
-3.17336E+00 -5.93368E-01 -5.93368E-01 -5.93368E-01
-2.75486E+00 -4.87845E-01 -4.87845E-01 -4.87845E-01
```

**.AMI File**

```plaintext
{Model_Specific
 (tap_filter (Description "Array of transmit de-emphasis tap
 (-1 (Usage in/out)(Range 0.0 -1.0 1.0)(Type tap)(Default
 (Description "Pre-cursor tap weight"))
 (0 (Usage in/out)(Range 1.0 -1.0 1.0)(Type tap)(Default
 (Description "Main tap weight"))
 (1 (Usage in/out)(Range 0.0 -1.0 1.0)(Type tap)(Default
 (Description "First post-cursor tap weight"))
 (2 (Usage in/out)(Range 0.0 -1.0 1.0)(Type tap)(Default
 (Description "Second post-cursor tap weight"))
 ) | End tap filter
 (tx_swing (Usage In)(Range 1.0 0.3 1.0)(Type float)(Default
 (Description "Peak differential output voltage")
```

**Algorithmic (.dll) Model**

| TX1:tap_filter-1 | Tap | AMI Range | 0 |
| TX1:tap_filter-0 | Tap | AMI Range | 0.675 |
| TX1:tap_filter-1 | Tap | AMI Range | -3 |
| TX1:tap_filter-2 | Tap | AMI Range | -0.025 |
6.25 Gbps Design Example

- Channel design questions
  - Which connectors?
  - Effect of tolerances?
  - Minimum link spacing?
  - Back-drilling?
  - Low-loss dielectric?

- SerDes IP questions
  - Equalization needed?
    - TX?
    - RX?
  - How many taps?
  - RX DFE needed?
  - Benefit of 8B10B encoding?
Channel Model & Design Decisions

Models
- IBIS-AMI Models
- S-Parameter Data
- Lossy Transmission Lines

Tolerances
- SerDes TX Process Voltage Temperature
- Packages Process
- PCB Traces Impedance Velocity
- SerDes RX Process Voltage Temperature

Design Decisions
- SerDes TX Tap settings Voltage swing
- Packages Breakout pattern
- PCB Traces Cross section Dielectric Spacing Via design
- Connector Vendor selection Breakout pattern
- SerDes RX Peaking filter mode DFE settings CDR settings
Network Characterization

- Analog circuit analysis includes TX output impedance/parasitics & RX input termination network
- Impulse response derived for use with algorithmic models
- Other network parameters may be extracted and displayed
  - S-parameters and transfer functions are shown in this example
Statistical Analysis

- Computes eye distributions / statistics directly
- Extremely fast – over $10^{15}$ equivalent bits/second
- Models linear TX/RX equalization
- Conceptually similar to many proprietary tools, but with vendor-specific SerDes IP models
Optimizing Transmitter Tap Settings

Tap settings to be investigated

<table>
<thead>
<tr>
<th>Tap</th>
<th>AMI Range</th>
<th>TX1:tap_filter.1 Tap</th>
<th>TX1:tap_filter.0 Tap</th>
<th>TX1:tap_filter.1 Tap</th>
<th>TX1:tap_filter.2 Tap</th>
<th>TX1:tx_swing Float</th>
<th>AMI Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMI Range</td>
<td>0</td>
<td>-0.05</td>
<td>-0.1</td>
<td>-0.2</td>
<td>-0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>1</td>
<td>0.9</td>
<td>0.7</td>
<td>0.7</td>
<td>0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>0</td>
<td>-0.1</td>
<td>-0.2</td>
<td>-0.4</td>
<td>0</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>0</td>
<td>-0.1</td>
<td>-0.2</td>
<td>-0.3</td>
<td>0</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>1.0</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td>0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>0.05</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td>0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>0.05</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td>0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>0.05</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td>0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI Range</td>
<td>0.05</td>
<td>0</td>
<td>0.7</td>
<td>0.7</td>
<td>0.3</td>
<td>0.8</td>
<td>0.7</td>
</tr>
</tbody>
</table>

64 permutations

Statistical Analysis

BER vs. TX tap settings

Statistical Eye @ RX
Time-Domain Analysis

- High-performance simulation
  - ~1,000,000 bits/minute
- Models non-linear effects
  - Decision Feedback Equalization (DFE)
- Models time-varying behavior
  - Auto-adaptation
  - Detailed clock recovery
- Models different encoding schemes and impact of worst-case pattern sequences
Equalization Configurations

No EQ: BER=0.030  Eye Margin = 0mV

TX EQ only: BER=0  Eye Margin = 36.8mV

RX EQ only: BER=1.26e-018  Eye Margin = 26.4mV

TX & RX EQ: BER=0  Eye Margin = 50.8mV
Modeling Adaptive Optimization

- RX DFE model includes adaptive equalization behavior, allowing model to optimize tap coefficients based on input data stream.
- Model outputs internal state (tap settings) information as simulation progresses.
- Tap behavior is saved in a format that can be loaded and displayed.
Simulation Performance

• Statistical Analysis
  – Simulating $10^{100}$ equivalent bits takes under 2 seconds
  – Hundreds of simulations can be run in a few minutes

• Time-Domain Analysis
  – Typical performance: 250K – 1M bits/minute, depending on model complexity
  – 10 million bit simulations are practical, billion bit simulations are possible

• IBIS-AMI models provide 500-10,000x the performance of traditional SPICE-based simulation

• IBIS-AMI models provide equivalent simulation performance to proprietary SerDes simulation tools
SPICE to IBIS-AMI Correlation

PCI Gen 1

PCI Gen 2

XAUI

Green = SPICE, Blue = IBIS-AMI
Where waveform is green, simulations match

IBIS-AMI and SPICE models provided by IBM
IBM HSSCDR to IBIS-AMI Correlation

Green = HSSCDR results, Blue = EDA Tool results using IBIS-AMI models
Where waveform is green, results are identical
Summary

• Systems designers need high-performance, interoperable SerDes IP models
• IBIS-AMI models are interoperable (mix different vendor models) and transportable (models run in different EDA tools)
• IBIS-AMI models support statistical analysis and time-domain simulation at ~1,000,000 bits/minute
• IBIS-AMI models have been correlated against multiple reference simulation environments
• IBIS-AMI models are available now!
Additional Slides
SPICE/EDA Tool Correlation Process

IBIS Analog, IBIS-AMI Models

EDA Tool

Test Pattern

SPICE Analysis

TX Model with EQ = ON
Channel Model
RX Model

IBIS-AMI Waveform

Reference Waveform
HSSCDR Correlation Methodology

EDA Tool