Agenda

• Review IBIS’s role in high-speed SI analysis, especially those new developments, from device modeling, interconnect modeling, and system level simulation automation perspectives.

• Discuss how IBIS as a standard, provides some of the leading technologies for the high-speed design, modeling and simulation industry; whereas in some areas, IBIS standards are lagging behind what industry is doing.

• Promote the thinking of what our current industry needs and what future technologies might bring us.
IBIS’s Role in High-Speed SI Analysis

Device Modeling

Interconnect Modeling

Package

Card

Board

System Level Simulation Automation
IBIS Evolution

IBIS Development

- Advanced Modeling Interface (AMI)
- Gate modulation support
- Current distribution support
- Added analog-only support (Verilog-A)
- Fixes for standardization
- Links to Verilog-AMS, VHDL-AMS and Berkeley SPICE files
- Differential thresholds, loads
- New meas. & delay loads
- Golden Waveforms and loads
- All IBIS 2.1 features plus
  - Package modeling
  - Series devices
  - Scheduled drivers

IBIS 5.0

IBIS 4.2*

IBIS 4.1

IBIS 4.0

IBIS 3.2*

IBIS 2.1

Reference: New Table-based Keywords in IBIS 5.0, Michael Mirmak, 2008 IBIS Summit China
IBIS Latest Status in 2009

- Device modeling enhancement
  - BIRDs for IBIS 5.0
    - BIRD74.6 – EMI Parameters
    - BIRD95.6 – Power Integrity Analysis using IBIS
    - BIRD97.2/98.1 – Gate Modulation Effect
    - BIRD103.1 – [Model Spec] DDR2 Over/Undershoot
    - BIRD104.1 – Algorithmic Modeling API
    - BIRD107.2 – Update to Algorithmic Modeling API
    - BIRD108 – Fixing Algorithmic Modeling API Impulse Matrix Nomenclature

- Interconnect modeling enhancement
  - Touchstone 2.0 completed and released
    - Sparse matrices and node-port matching now under development
    - Parser development about to begin
IBIS Device Modeling - AMI Development
IBIS AMI Device Model Key Concepts

- Device models for high-speed channel simulations that need sophisticated FFE and DFE algorithms
  - The Tx –to– Rx pathway is composed of 3 separate entities
    - Tx algorithmic part, Analog channel, Rx algorithmic part

- Model delivered as a dynamically linked library (DLL)
  - Executable models contain and conceal IC company’s advanced device algorithms
Observations

- IBIS AMI, a novel idea and technical approach that meets current and future modeling and simulation needs, and also fits the business model for IC company (who provides) and system company (who uses)

- IC technology advances fast, which requires more advanced IBIS AMI models beyond current standard to support existing designs

- The provided IBIS AMI models from some IC Companies are just part of the product line, not complete

- Many IC companies are yet to have the practice or know-how to deliver IBIS AMI models
Advanced feature needed - Cascaded AMI

DSP blocks for signal conditioning and clock and data recovery

Cascaded AMI → Allows flexible Modeling and debug
Example: cascade equalizer model with stand alone CDR
Advanced feature needed: Xtalk aware

- Standard IBIS AMI models are only required to filter the main channel.
- Advanced AMIFFE models will optimize the filter coefficients for the main channel, and has the capability to filter the xtalk channel using those coefficients.
Advanced IBIS AMI Function Blocks

Advanced AMI implementations with highly customizable configurations can model the real world devices

- AMI CDR2 – Stand alone clock data recovery
- AMI FFE – Feed forward filter model (tap optimization)
- AMI CTF – Analog filter model
- AMI DFE – DFE with blind adaption
- AMI DFENL – DFE with look ahead equalizer
Beyond IBIS AMI - Hybrid Model Support

• IBIS-AMI
• IBIS with driver schedule
• HSPICE/Encrypted HSPICE
• Verilog-A
• IC companies’ proprietary models (C or Matlab based), such as those in IBM HSSCDR
Beyond IBIS AMI - Non-Ideal PDS SI Analysis

AMI models can be powered through real PDS

*Disable ideal PDS

Input power at VRM location of PCB

Red: non-ideal Power shows more noisy eye
High-speed Gigabit Serial Simulation with AMI models (2.5Gbps Vs 5Gbps)

Eye Contour

Bathtub
High-speed Gigabit Serial Simulation with AMI models (2.5Gbps Vs 5Gbps)
IBIS Interconnect Modeling - S Parameters
Package RLC models, EBD and S Parameters

- **IBIS PKG** (IC Package Model) RLC (per pin matrix) is OK for electrical short structures such as IC packages and the frequency response is needed within a few GHz. See reference paper at IBIS Shanghai 2006 [http://www.vhdl.org/pub/ibis/summits/oct06a/chitwood.pdf](http://www.vhdl.org/pub/ibis/summits/oct06a/chitwood.pdf)

- **IBIS EBD** (Electrical Board Description) is designed for electrical long structures but the lack of coupling and return path descriptions makes it unsuitable for high-speed SI. See reference paper at IBIS Shanghai 2008 [http://www.vhdl.org/pub/ibis/summits/nov08a/xu.pdf](http://www.vhdl.org/pub/ibis/summits/nov08a/xu.pdf)

- **S-Parameter**
  widely used for accurate high frequency simulation, though has its own issues, is the most popular for interconnect model. See reference paper at IBIS Shanghai 2008 [http://www.vhdl.org/pub/ibis/summits/nov08a/huang.pdf](http://www.vhdl.org/pub/ibis/summits/nov08a/huang.pdf)
IBIS Touchstone ver2.0 for S-Parameters

- Complete backward compatibility with Touchstone 1.0, released in July 2009.

- Mixed-mode support (single ended + diff. signals), which enables SI analysis with the impact of the PDS

- Per-port impedance references. This facilitates power to signal port modeling of coupling and Power Integrity simulation.

- Removal of upper limits on number of data points and number of ports. This facilitates modeling of large ICs.

- Some minor fixes and clarifications. In Touchstone 1.0, Z and Y were normalized with respect to Z0. In Touchstone 2.0, Z and Y are non-normalized and independent of Z0.

Beyond Touchstone 2.0

- For a large S matrix (model for many signal and/or power/ground nets), the Touchstone data file could be huge (few hundreds of MB)

- New format under IBIS task team investigation – Pole/Zero format
  - Extreme compact, only store poles and residues for the rational function approximation
  - Highly efficient simulation, using recursive convolution
  - S-parameter data are stored as vector fitted curve so it is an approximation

- Proprietary format – Sigrity BNP API for S-parameter
  - Very Compact and extremely accurate
  - Do not store tabulated data, provides raw data on demand
Current Simulation Flow

- Through TouchStone (TS) S-parameter file
Proprietary Flow for Enhanced Integration

- Frequency domain data exchange through API with broadband response
  - BNP data file does *not* store the frequency data points as does in a Touchstone file. It calculates any requested frequency point whenever the API is called within the simulation band. Therefore, the need to interpolate S-parameter tabulated data is completely eliminated. Since the API transports raw data, no pole/zero approximation needed.
S-Parameter Usage Example

Using S-Parameter in both TouchStone and BNP formats in HSPICE

```
.model Smodel_name S TSTONEfile=file or BNPfile=file
```

TS file: xyz.snp   BNP file: xyz.bnp

BNP file is much smaller than TS file, but yields higher simulation accuracy and convergence

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Freq #</th>
<th>Touchstone File</th>
<th>Touchstone File Zipped</th>
<th>BNP File</th>
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High-speed 1066Mbps Source Synchronous Simulation (BNP Vs Touchstone)

- VCC Power @ Die waveform with BNP Vs Touchstone model
- BNP model simulation has higher efficiency, better convergence and accuracy
High-speed 1066Mbps Source Synchronous Simulation (BNP Vs Touchstone)

- DQ @ Board waveform with BNP Vs Touchstone model
- BNP model simulation has higher efficiency, better convergence and accuracy
Summary

- Reviewed IBIS device model - AMI and its support
- Reviewed S-parameter as the interconnect model, introduced IBIS Touchstone 2.0 and Sigrity BNP
- Next review will be on how device models and interconnect models are connected for system level simulation automation.
Thank You!