System Simulation Automation
- Model Connection Review

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Agenda

- Discuss concepts related to electrical model connectivity for chip/package/board system-level analysis
- Review existing solutions
  - no standards exist
    - some existing solution specifications are under NDA
  - An example protocol specification and physical example
- Summary

NOTE:
- The Sigrity model connection protocol discussed in this presentation is not being proposed as a standard, merely as an example of an existing solution created in reaction to short term need and lack of existing standard protocols.
Challenge for Chip/Package/Board, Signals and Power/Ground Simulation

- Assume I have …
  - a chip/package/board system with hundreds or thousands of physical connections (pins)
  - individual electrical models for each chip, package and board

- How do I …
  1. know which pins of one model to connect to the pins of another model?
  2. reliably and in reasonable time connect these models in a netlist or a schematic?
Observations

- Pin section and pin mapping sections in IBIS model are used to connect packages to PCBs, and IBIS EBD pins are used to connect DIMM modules to PCB...these enable all EDA tools to do system level simulation in the past decade.

- IBIS does not provide die (chip) side connectivity and die side model.
- IBIS provides physical pin information, but not physical pin to circuit node mapping for model abstraction.
- IBIS provides connectivity for I/O, but not much information on the signal return paths – the power/ground network.
Requirements

- **Chip/package/board systems have many physical connections (pins)**
  - chip-package boundary \(\approx 100 – 5000\)
  - package-board boundary \(\approx 100 – 2000\)

- **Not all electrical models can have pin-level resolution**
  - models may be too large to compute, store, etc.
  - difficult to connect in EDA tools

- **Adequate modeling may not be possible with net-level resolution**
  - especially, if this low resolution is applied throughout the entire system
  - NOTE: “net-level resolution” groups all pins for each net at a domain boundary

- **Support is required for**
  - arbitrarily pin-grouped models
  - automated connection amongst models in EDA tools
System Analysis

Physical connectivity

Chip-centric model abstraction

Board-centric model abstraction
System Analysis

- A bit more detailed view of electrical model resolution through pin grouping, for one domain boundary
modern system designs requires various levels of model resolution throughout the system, with pin-level, net-level and arbitrarily grouped pins applied to the same component.
Existing Model Connection Protocols for Chip/Package/Board Analysis

- **Sigrity MCP (Model Connection Protocol)**
  - defined by Sigrity
    - publicly available definition
  - objective to support chip/package/board system analysis

- **Apache CPP**
  - defined by Apache
    - definition covered under NDA

- Implemented as “headers”
- Contained within model-native comment lines
  - model could be either subcircuit or data file
A Typical Model Connection Protocol
(Sigrity MCP)

* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] {DIE|PKG|PCB}
* [MCP Source] source text
* [Coordinate Unit] unit
* [Connection] connectionName partName numberPhysicalPins
  * [Connection Type] {DIE|PKG|PCB}
  * [Power Nets]
  * pinName modelName netName x y
  * ...
  * pinName modelName netName x y
  * [Ground Nets]
  * pinName modelName netName x y
  * ...
  * pinName modelName netName x y
  * [Signal Nets]
  * pinName modelName netName x y
  * ...
  * pinName modelName netName x y
  * [MCP End]
A Typical Model Connection Protocol

- Only one instance of [Structure Type]

- Multiple instances of [Connection] are possible
  - for a single-die package there will be one die-type connection and one pcb-type connection
  - for a pcb there may be many package type connections
  - for a multi-die SiP package there may be multiple die-type connections

- Only one instance of [Connection Type] per [Connection]

- For power integrity applications there may be no signal nets in the model

- Not all physical pins must be documented, only those included in the electrical model
  - For power integrity applications there may be no signal nets
  - For Touchstone data files there may only be signal nets
    - the reference terminal is implicit for the data file
  - For SPICE subcircuits there are likely grounds net but maybe no power nets
    - the reference terminal must be explicit
A Physical Example

- a few nets in a small 4-layer flipchip BGA package
  (so the MCP sections fin on a single page)
  - 3 power nets
  - 1 ground net
  - 2 signal nets
12-by-12 bump and ball arrays
(for active nets)
Model Resolution

- **pin-level at the chip-package boundary**
  - 36 physical pins - 36 electrical nodes
    - 18 power nodes - 5 VDD_1, 5 VDD_4, 8 VDDcore
    - 16 ground nodes - 16 VSS
    - 2 signal nodes - Net_1, Net_2

- **net-level at the package-board boundary**
  - 36 physical pins - 6 electrical nodes
    - 3 power nodes - 1 VDD_1, 1 VDD_4, 1 VDDcore
    - 1 ground nodes - 1 VSS
    - 2 signal nodes - Net_1, Net_2
Model Extraction Setup

- die-side setup for pin-level model extraction
- board-side setup for net-based model extraction
  - equivalent to pin-level model extraction with 1-by-1 grid-based pin grouping
A Typical Package
(one power net)
A SPICE circuit with MCP header
(a mixed pin-level/net-level model)

.SUBCKT FlipChip_pkg_SPICE
+ U1_E3 U1_F1 U1_F2 U1_F3 U1_G3
+ U1_K6 U1_K7 U1_L6 U1_L7 U1_M6
+ U1_D4 U1_D9 U1_E4 U1_E9 U1_H4 U1_H9 U1_J4 U1_J9
+ U1_A1 U1_A12 U1_B11 U1_B2 U1_E5 U1_E8 U1_F7 U1_G6
+ U1_G7 U1_H5 U1_H8 U1_L11 U1_L2 U1_M1 U1_M12 U1_F6
+ U1_L1 U1_K1
+ BGA1_C1 BGA1_K6 BGA1_C10 BGA1_A1 BGA1_L2 BGA1_J3
*

* The following is the Sigrity MCP Section
***********************************************************************************************************************
*[MCP Begin]
*[MCP Ver] 1.0
*[Structure Type] PKG
*[MCP Source] Sigrity XtractIM 3.0.2.07061 7/18/2009
A SPICE circuit with MCP header
(a pin-level die-side connection)

* [Connection] U1 die_12x12 144
* [Connection Type] DIE
* [Power Nets]
  * E3  U1_E3   VDD_1
  * F1  U1_F1   VDD_1
  * F2  U1_F2   VDD_1
  * F3  U1_F3   VDD_1
  * G3  U1_G3   VDD_1
  * K6  U1_K6   VDD_4
  * K7  U1_K7   VDD_4
  * L6  U1_L6   VDD_4
  * L7  U1_L7   VDD_4
  * M6  U1_M6   VDD_4
  * D4  U1_D4   VDDcore
  * D9  U1_D9   VDDcore
  * E4  U1_E4   VDDcore
  * E9  U1_E9   VDDcore
  * H4  U1_H4   VDDcore
  * H9  U1_H9   VDDcore
  * J4  U1_J4   VDDcore
  * J9  U1_J9   VDDcore
A SPICE circuit with MCP header
(a pin-level die-side connection)

* [Ground Nets]
  * A1  U1_A1  VSS
  * A12 U1_A12 VSS
  * B11 U1_B11 VSS
  * B2  U1_B2  VSS
  * E5  U1_E5  VSS
  * E8  U1_E8  VSS
  * F7  U1_F7  VSS
  * G6  U1_G6  VSS
  * G7  U1_G7  VSS
  * H5  U1_H5  VSS
  * H8  U1_H8  VSS
  * L11 U1_L11 VSS
  * L2  U1_L2  VSS
  * M1  U1_M1  VSS
  * M12 U1_M12 VSS
  * F6  U1_F6  VSS

* [Signal Nets]
  * L1  U1_L1  Net_1
  * K1  U1_K1  Net_2
A SPICE circuit with MCP header
(a net-base pcb-side connection)

* [Connection] BGA1 board_12x12 144
* [Connection Type] PCB
* [Power Nets]
  * C1 BGA1_C1 VDD_1
  * F3 BGA1_C1 VDD_1
  * G1 BGA1_C1 VDD_1
  * G3 BGA1_C1 VDD_1
  * K1 BGA1_C1 VDD_1
  * K6 BGA1_K6 VDD_4
  * K7 BGA1_K6 VDD_4
  * M10 BGA1_K6 VDD_4
  * M3 BGA1_K6 VDD_4
  * M7 BGA1_K6 VDD_4
  * C10 BGA1_C10 VDDcore
  * C3 BGA1_C10 VDDcore
  * D4 BGA1_C10 VDDcore
  * D9 BGA1_C10 VDDcore
  * J4 BGA1_C10 VDDcore
  * J9 BGA1_C10 VDDcore
  * K10 BGA1_C10 VDDcore
  * K3 BGA1_C10 VDDcore

VDD_1
VDD_4
VDDcore

a single electrical node
A SPICE circuit with MCP header
(a net-level pcb-side connection)

* [Ground Nets]
  * A1  BGA1_A1  VSS
  * A12 BGA1_A1  VSS
  * A5  BGA1_A1  VSS
  * A8  BGA1_A1  VSS
  * E1  BGA1_A1  VSS
  * E12 BGA1_A1  VSS
  * F6  BGA1_A1  VSS
  * F7  BGA1_A1  VSS
  * G6  BGA1_A1  VSS
  * G7  BGA1_A1  VSS
  * H1  BGA1_A1  VSS
  * H12 BGA1_A1  VSS
  * M1  BGA1_A1  VSS
  * M12 BGA1_A1  VSS
  * M5  BGA1_A1  VSS
  * M8  BGA1_A1  VSS
  * [Signal Nets]
  * L2  BGA1_L2  Net_1
  * J3  BGA1_J3  Net_2
  *
  * [MCP End]
A Channel Connection

- The channel is comprised of one transmitter, one receiver, a printed-circuit board or PCB and two packages
- MCP is used to maintain the connections between blocks
Summary

- Chip/package/board designs may have thousands of pins
- Chip/package/board system analysis requires
  - user-definable model resolution
  - automated connection support for EDA tools
- Circuit and data models are commonly applied
  - both should be supported by any connection protocol
- Model connection protocols are much more than simply “port names”
- Proprietary model connection protocols are currently being applied
- An industry standard model connection protocol should be defined
  - user and EDA vendor participation will be required to agree on a standard
  - active participation by more than a few individuals will be required
Thank You!