Application of Model Connection Protocols for System-level Power Delivery Network Analysis

IBIS Summit
Tokyo, Japan
November 6, 2009

Yutaka Honda, ATE Service Corp. yutaka@ate.co.jp
Brad Brim, Sigrity Inc. bradb@sigrity.com
**Agenda**

- Discuss chip/package/board system-level analysis
- Review connectivity protocols
- A power delivery network example

**NOTE:**
- The Sigrity model connection protocol discussed in this presentation is not being proposed as a standard, merely as an example of an existing solution created in reaction to short term need and lack of existing standard protocols.
System-level analysis challenges (1)

Assume I have …

- a chip/package/board system with thousands of physical pins
- individual models for chip, package, board

A Package Bump Map
(1500 pins for *only* VCC)

2D/3D inductance map
System-level analysis challenges (2)

How do I …

1. know which pins of one model to connect to the pins of another model?
2. reliably and quickly connect these models in a netlist or schematic?
Requirements

- Chip/package/board systems have many physical connections (pins)
  - chip-package boundary \(\approx\) 100 – 6000
  - package-board boundary \(\approx\) 100 – 2500

- Not all electrical models can have pin-level resolution
  - models may be too large to compute, store, etc.
  - difficult to connect in EDA tools

- Adequate modeling may not be possible with net-level resolution
  - especially, if this low resolution is applied throughout the entire system
    - NOTE: “net-level resolution” groups all pins for each net at a domain boundary

- Support is required for
  - arbitrarily pin-grouped models
  - automated connection amongst models in EDA tools
System Analysis

Chip-centric model abstraction

Board-centric model abstraction

Physical connectivity
Existing Model Connection Protocols for Chip/Package/Board Analysis

- **Sigrity MCP (Model Connection Protocol)**
  - defined by Sigrity
    - publicly available definition
  - objective to support chip/package/board system analysis
  - version 1.1 available with user-requested pin locations for support where pin name mismatches exist

- **Apache CPP**
  - defined by Apache
    - definition covered under NDA

- Implemented as model “headers”
- Contained within model-native comment lines
  - model could be either subcircuit or data file
A Typical Model Connection Protocol  
(Sigrity MCP)  

* [MCP Begin]  
* [MCP Ver] 1.1  
* [Structure Type] {DIE|PKG|PCB}  
* [MCP Source] source text  
* [Coordinate Unit] unit  
* [Connection] connectionName partName numberPhysicalPins  
  * [Connection Type] {DIE|PKG|PCB}  
  * [Power Nets]  
  * pinName modelNodeName netName x y  
  * ...  
  * pinName modelNodeName netName x y  
  * [Ground Nets]  
  * pinName modelNodeName netName x y  
  * ...  
  * pinName modelNodeName netName x y  
  * [Signal Nets]  
  * pinName modelNodeName netName x y  
  * ...  
  * pinName modelNodeName netName x y  
* [MCP End]
Example chip-package-board system

- **Goal**
  - reduce/eliminate PDN impedance peaks at the chip

- **Requirements**
  - avoid a board re-spin
    - use existing stack-up
    - use existing decap locations
    - allow only same-size or smaller decaps
  - performance is primary, cost is secondary
    - allow more expensive decaps if required
Example chip-package-board system

- 400 VDD bumps
- 2007 VSS bumps

- 98 VDD balls
- 227 VSS balls

10-layer BGA package

24-layer Board
Example chip-package-board system

*initial decap placement*

- **220 capacitors**
  - in-package: 4
  - core area: 98
  - close to device: 109
  - VRM bulk caps: 9
System PDN analysis setup

1) Merged board-package analysis
   - per-net chip model
   - per-pin connectivity between board and package

2-1) Analysis with pin-grouped package model
   - per net chip model
   - Grouped (4-by-4 grid) connectivity between board and package
     - 32 electrical connections – 16 VDD, 16 VSS

2-2) Optimization of PDN for performance and cost
   - same setup as 2-1) above
System analysis with merged board/package

- 4 hours simulation time
- 5GB RAM
- 180% of $Z_{\text{target}}$ at peak
- Cost = 4.6

**NOTE:**
- 24-layer board and 10-layer package databases are merged into single design.
- Per-pin connection between board and package with all couplings.
Concept of the Model-to-Model Link by MCP

- **Chip**
  - On-die circuit netlist
  - MCP * [connection type] PKG
  - MCP * [connection type] DIE

- **Package**
  - Package SPICE netlist / S-parameter
  - MCP * [connection type] PCB

- **Board**
  - Board geometry model / S-parameter
  - MCP * [connection type] PKG
EDA mapping of the MCP package model

define an MCP model link

(1) select the model type

(2) choose a file

(3) select the connection

NOTE:
- 3 mouse clicks associate an external model with the component definition.
- Quick and error-free process.
System analysis with pin-grouped package model

- **Package Model**
  - S-parameters - 2 hours, 3GB RAM
  - RLCK model - 30 minutes, 3GB RAM

- **Board** (with package model attached)
  - 10 minutes, 1GB RAM

**NOTE:**
- 24-layer board simulated with S-parameter model for package.
- 4-by-4 board/package connection.
System optimization with pin-grouped package model

- 40 minutes optimization time
- 65% of $Z_{\text{target}}$ at switching frequencies
- Cost = 2.3 (50% savings) with 93 decaps

**NOTE:**
- board analysis results are re-used.
System optimization with pin-grouped package model

PDN performance (associated with impedance)

Success!
- Impedance peaks have been eliminated
- Impedance is less than $Z_{\text{target}}$ over frequency range of interest
- Decap cost is saved as well

89 board decaps
4 in-package decaps
Observations

- Chip/package/board designs may have thousands of pins
- Chip/package/board PDN system analysis and optimization requires
  - user-definable model resolution
  - automated connection support for EDA tools

- Circuit and data models are commonly applied
  - both should be supported by any connection protocol
- Model connection protocols are much more than simply “port names”
- Proprietary model connection protocols are currently being applied

- An industry standard model connection protocol should be defined
  - user and EDA vendor participation will be required to agree on a standard
  - active participation by more than a few individuals will be required
  - the authors intend to escalate this topic with the IBIS committees
    - many designers and EDA vendors need as soon as possible
Thank You!