Model Connection Protocol
extensions for Mixed Signal SiP

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Agenda

- Why Model Connection Protocol
- Model Connection Protocol overview
- Extensions required for Mixed Signal SiP
- MCP Applications
- Summary
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design

- Design low impedance path: supply to chip

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Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design

Chip PDN models can vary from 2-node to N-nodes, where N is the number of physical pins.

There can be 1 to M current sources, where M may be much larger than N.
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design

- Chip/Package/Board have many physical connections
  - Chip-Package Boundary: 100-6000
  - Package-Board Boundary: 100-3000

- Not all electrical nodes can have per-pin resolution
  - Models may become too large for computation, simulation

- Need way to group pins and auto-connect models across IC/Pkg/Board
MCP Overview

- Establish mapping

Pin grouping and mapping
- physical pin (of layout) to electrical node (of model) per Net
- Mapping to connecting structure using physical location

Example of VDD net across chip-pkg-board
MCP Overview

- Establish mapping

Example of VDD net across chip-pkg-board

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MCP Extensions for Mixed Signal SiP

- Analyze power-delivery to ICs when Package rails supply power to
  - different ICs that could be digital and/or analog
  - RF-modules and Passive/Active SMDs

- Need Schematic driven Mixed Signal Simulations to process IR-drop at power-rails
MCP Extensions for Mixed Signal SiP
-Current MCP scope

Board ➔ Package ➔ DIE-Digital
MCP Extensions for Mixed Signal SiP

Board  Package  DIE-Analog  DIE-Digital
Module (Example RFmodule, SMDs)
MCP Extensions for Mixed Signal SiP
- Mixed Signal IR-drop Task Flow

Schematic driven Analog

SiP & Circuit Design
Schematic Capture

Pre- & Post-Layout Simulation

Passive Structures

SiP Layout

Power-RAIL extract

Analog IC Layout

Power-Net Extract

Analog IR-drop
(schematic simulation driven)

Digital IR-drop

HDL

Digital IC layout

Power-Net Extract

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Support for mapping of different electrical port-groups across different structures

- As an example
  - a package model with 2-by-2 grid-based pin grouping
  - a chip model with 3-by-3 grid-based pin grouping

- desired is an electrical circuit to interface between an 8 node circuit and an 18 node circuit
MCP Extensions for Mixed Signal SiP

- Optional Column for mapping of electrical nodes across structures

Package: .Subckt bp1 dp1

Board

<table>
<thead>
<tr>
<th>Pin</th>
<th>VDD</th>
<th>5 4</th>
<th>D1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin2</td>
<td>VDD</td>
<td>6 4</td>
<td>D1A</td>
</tr>
<tr>
<td>Pin3</td>
<td>VDD</td>
<td>7 4</td>
<td>D1A</td>
</tr>
<tr>
<td>Pin4</td>
<td>VDD</td>
<td>8 4</td>
<td>D1B</td>
</tr>
<tr>
<td>Pin5</td>
<td>VDD</td>
<td>9 4</td>
<td>D1B</td>
</tr>
</tbody>
</table>

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MCP Extensions for Mixed Signal SiP
- Caution: Electrical connectivity with disparate pin grouping

- Examine the nodes of the each net
  - for overlapping pin group domains, the corresponding nodes are shorted together
    - (1,1) node shorts together \{(1,1), (1,2), (2,1), (2,2)\} nodes
    - (1,2) node shorts together \{(1,2), (1,3), (2,2), (2,3)\} nodes
    - (2,1) node shorts together \{(2,1), (2,2), (3,1), (3,2)\} nodes
    - (2,2) node shorts together \{(2,2), (2,3), (3,2), (3,3)\} nodes
    - alternately
      - (2,2) node shorts together \{(1,1), (1,2), (2,1), (2,2)\} nodes
  - all nodes are shorted together, reducing to per-net connectivity
    - instead of 8 or 18 node electrical connectivity it is actually 2 node connectivity

- Recommendation
  - Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains
    - but it can reduce the effective resolution of the model at the chip/package interface
    - Useful in case of early debugging and quick connectivity

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Extensions over existing MCP
- Support for Modules as connect type structures

- Mixed Signal SiPs would have elements other than ICs like
  - RF modules
  - Metal Passive structures
  - SMD components
  - Silicon Interposers

- These structures draw power impacting PDN loading and hence we need to support [Module] category besides IC, Package and Board
Extensions over existing MCP

- Support for Modules as connect type structures
In order to connect to structures that are SMD or metal-passive structures on SiP – usually a case for Mixed Signal SiP, it becomes difficult to connect by X-Y locations.

Early analysis may require quick way of stitching the models across structures and minor placement or resolution changes can cause X-Y mapping to fail.

Optional column showing connection by REFDES makes easy mapping for Mixed-Signal modules and early trials

Examples of connecting interfaces could be

- IO-cellname (DIE IO)
- R1:1 (pin 1 of R1)
- CONN:1 (pin1 of PCB connector)
- my_model_opamp:3 (port-3 of opamp subcircuit)
Extensions over existing MCP
- Connection by Refdes besides X-Y location

- Simulating Analog DIE in package schematics with loading from passive structures connected to DIE

- The simulation data is post-processed to obtain IR-drop at power-rails

[connection type MODULE]

<table>
<thead>
<tr>
<th>Pin1</th>
<th>dp1</th>
<th>VDD</th>
<th>5 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin2</td>
<td>dp1</td>
<td>VDD</td>
<td>6 4</td>
</tr>
<tr>
<td>Pin3</td>
<td>dp1</td>
<td>VDD</td>
<td>7 4</td>
</tr>
</tbody>
</table>

varistor1:2 //Reference_design:pin//
varistor2:2
MCP applications: Digital DIE IR-drop
- Digital DIE in context of package model

Simulation results of Vdd rail: Dynamic IR-Drop

Without package effects
worst-case IR drop: 147.5mV

With package effects
worst-case IR drop: 179.3mV
MCP applications: Analog DIE IR-drop
-Analog DIE in context of package model & Digital DIE-models

- Analog DIE test-bench with power-rail model
- Digital DIE model connected to represent loading of power-rail
- Analog DIE IR-drop post simulations
Summary: MCP format updated in context of Mixed Signal contents