Extending/Leveraging IBIS Constructs to Model High-Speed I/Os and Packages using AMI, Spice, and S-Parameters

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Agenda

• IBIS Overview

• Why extend IBIS to SPICE models
  – Current Limitations

• Leveraging [External Model] to allow including Package S-Parameters for High Speed simulation
  – Example

• Extending [External Model] to:
  – Simulate VI-VT model in conjunction with Spice sub-circuits that represent RDL elements, DSP Spice code, etc.
  – Dynamically switch sub-circuits to take care of corners and parametric variations.
  – Simulate AMI with [External Model] that represents analog IO modeled in Spice or S-parameters.

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• Summary
IBIS overview

- Analog IO model is modelled by IBIS VI and VT curves
- Equalization (DSP algorithmic) portion of IO model is modelled by AMI C-code (Algorithmic Model Interface) that is pointed by IBIS model
- RDL and or pin parasitics are lumped into pin R/L/C values
Why extend IBIS to SPICE models

• At high frequencies, IO buffers could have portions that need to be modeled using Spice files:
  – On DIE Terminations (ODT) that vary with frequencies need to be expressed as s-parameters or RLGC Spice files
  – On DIE RDL parasitics become significant and vary with frequencies and hence have to be expressed as s-parameters or SPEF
  – Analog portion of IO-buffer is expressed as Spice as against VI-VT curve; s-parameters can also be used to describe transfer characteristics of IO-buffer amplifiers.
  – Some algorithmic portion may be modeled in Spice as against AMI code
Why extend IBIS to SPICE models

• Multiple Sub-circuits / Spice files
  – Different Spice sub-circuits could be applicable for different process corners. On-DIE RDL could be expressed as different s-parameter files for typ/min/max conditions.
  – Different Spice sub-circuits could be applicable for different buffer configurations. For example, Pre-emphasis portion could have been modeled as Spice using different sub-circuits for different settings.
  – ODT could be a function of current being drawn out of IO-buffer (Dynamic ODT) and could have been expressed as behavioral Spice, Verilog-A
Current Approach and Limitations

- Package parasitics can be used as S-parameters by including them as part of interconnect network in a way similar to external interconnect parasitics.
  - Limitation
    - RDL parasitics that need to be part of IO-buffer characterization are treated as interconnects and assumed bi-directional.
- Spice IO-buffers can be included as part of IBIS using [External Model] Keyword.
  - Limitations
    - Cannot model DSP (in SPICE) in conjunction with AMI model
      - Use of [External Model] in conjunction with VI-VT (IBIS) is not recommended today
    - Does not directly support s-parameters (Touchstone)
      - For example, it is not easy to model RDL and other elements in conjunction with VI-VT curves cannot take care of process corners and parametric selection of subcircuits
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• Summary
Leveraging [External Model] to Support Package S-Parameters

• Long-term: IBIS model should have Keywords to support Touchstone S-parameters under Package section, with fields to
  – point to touchstone file from the Package section
  – provide port-mapping of IO-buffer pins to s-parameter ports
  – R/L/C values should be ignored by SI tools if s-parameter file is used

• Short-term: This can be achieved through use of [External Model] keyword
  – Set R/L/C values in package keyword as ZERO (to avoid double counting)
  – Point to the touchstone file of the package inside the Spice subcircuits
Example: Support for S-parameters for package parasitics using [External Model]

- Use IBIS Device with 4 pins (1, 2, 3, and 4)

- Pins 1 and 2 are +ve and -ve diff pins respectively, with a “tx” diff model assigned to both of them

- Pins 3 and 4 are +ve and -ve diff pins respectively, with a “rx” tdiff model assigned to both of them

- Tx and Rx contain corresponding
  - [External Model] section
Example ....

- Set the values of all package parasitics to 0 or NA because in this case we will model the package using an s-parameter that is referenced from the Rx/Tx subckts.

- Assign the same model to each diff pin (e.g., tx is assigned to pins 1 and 2).

- Define the diff pins (e.g., 3 and 4) and specify vdiff.

Make values zero or NA

<table>
<thead>
<tr>
<th>Component</th>
<th>MyComp</th>
<th>Manufacturer</th>
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<tr>
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<table>
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<th>typ</th>
<th>min</th>
<th>max</th>
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<td>R_pkg</td>
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<td>0.0m</td>
<td>0.0m</td>
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<tr>
<td>L_pkg</td>
<td>0nH</td>
<td>0nH</td>
<td>0nH</td>
<td></td>
</tr>
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<td>C_pkg</td>
<td>0pF</td>
<td>0pF</td>
<td>0pF</td>
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<table>
<thead>
<tr>
<th>Pin</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
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<tr>
<td>1</td>
<td>OUT1</td>
<td>tx</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<td>2</td>
<td>OUT2</td>
<td>tx</td>
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<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>3</td>
<td>IN1</td>
<td>rx</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>4</td>
<td>IN2</td>
<td>rx</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<tr>
<th>Diff Pin</th>
<th>inv_pin</th>
<th>vdiff</th>
<th>tdelay_typ</th>
<th>tdelay_min</th>
<th>tdelay_max</th>
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<tr>
<td>1</td>
<td>2</td>
<td>200mV</td>
<td>0ns</td>
<td>0ns</td>
<td>0ns</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>200mV</td>
<td>0ns</td>
<td>0ns</td>
<td>0ns</td>
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</table>
Example ....

[External Model]
Language SPICE

<table>
<thead>
<tr>
<th>Corner</th>
<th>corner_name</th>
<th>file_name</th>
<th>circuit_name (.subckt name)</th>
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</thead>
<tbody>
<tr>
<td>Corner</td>
<td>Typ</td>
<td>tdiff_tx.spc</td>
<td>tdiff_tx_typ</td>
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<tr>
<td>Corner</td>
<td>Min</td>
<td>tdiff_tx.spc</td>
<td>tdiff_tx_min</td>
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<tr>
<td>Corner</td>
<td>Max</td>
<td>tdiff_tx.spc</td>
<td>tdiff_tx_max</td>
</tr>
</tbody>
</table>

| Ports List of port names (in same order as our 8-term macromodel) |
|Ports A_puref A_signal_pos A_pdref my_drive my_enable |
|Ports A_puref A_goref A_signal_neg my_ref |

D_to_A d_port port1 port2 vlow whigh trise tfall corner_name
D_to_A D_drive my_drive my_ref 0.0 3.3 0.5n 0.3n Typ
D_to_A D_drive my_drive my_ref 0.0 3.0 0.6n 0.3n Min
D_to_A D_drive my_drive my_ref 0.0 3.6 0.4n 0.3n Max

- Specify language as SPICE
- Specify the SPICE files that contain the subckts for the typ/min/max corners i.e., tdiff_rx.spc in this case;
- tdiff_rx.spc should contain the following subckts tdiff_rx_typ, tdiff_rx_min, and tdiff_rx_max
- Ports can be split on separate lines, but each line is a continuation for the previous one (in this case each subckt has 9 ports)
- Add the D/A or A/D statements (no need for D_enable and D_Drive conversion for input models)
The SPICE subckt tdiff_tx_typ for the typical corner in tdiff_tx.spc is as shown on the left. Min and Max similar.

We need to connect the extra IBIS nodes inside the subckt to make sure there are no disconnected nodes in the circuit.

This is a simple pass-through driver that applies the “in” stimulus and its inverted pattern to the package input nodes.

The s-parameter file (diff_pkg.dat) for the package is referenced internally in the subckt and connects the in and inv stimulus to the I/O output nodes i.e. 2 and 8.

Similar for Rx
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  - Simulate AMI with [External Model] that represents analog IO modeled in Spice or S-parameters.
- Summary
Simulate VI-VT model in conjunction with Spice

- Traditionally [External Model] keyword has been used for IO-buffer that needs to characterized as Spice IO in which case IBIS VI-VT data is not required.

- Extend use of [External Model] keyword to point to Spice sub-circuits that augment VI-VT data for complete characterization of IO-buffer.
  - Model On-DIE RDL parasitics using Spice or S-parameters that connect to Analog IO-buffer characterized as VI-VT data
  - Model DSP algorithm in Spice that works in conjunction with VI-VT data
Simulate VI-VT model in conjunction with Spice

[External Model]
Language **SPICE** | **SPARAM**
Type **Other**

<table>
<thead>
<tr>
<th>corner</th>
<th>file_name</th>
<th>circuit_name</th>
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<tbody>
<tr>
<td>Typ</td>
<td>dsp.spc</td>
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<td>Min</td>
<td>dsp.spc</td>
<td>dsp_min.s4p</td>
</tr>
<tr>
<td>Max</td>
<td>dsp.spc</td>
<td>dsp_max.s4p</td>
</tr>
</tbody>
</table>

| Ports List of port names (in same order as in SPICE | SPARAM) |
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
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• Summary
Dynamically switch sub-circuits to take care of corners and parametric variations.

[External Model]
Language SPICE

<table>
<thead>
<tr>
<th>corner</th>
<th>file_name</th>
<th>circuit_name</th>
<th>switch_param</th>
<th>switch_param_val</th>
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</thead>
<tbody>
<tr>
<td>Typ</td>
<td>tdiff.spc</td>
<td>tdiff_txrx_typ</td>
<td>temp</td>
<td>50, 100, 150</td>
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<tr>
<td>Typ</td>
<td>tdiff.spc</td>
<td>tdiff_txrx_typ</td>
<td>freq</td>
<td>1, 2, 5</td>
</tr>
<tr>
<td>Min</td>
<td>tdiff.spc</td>
<td>tdiff_txrx_min</td>
<td>temp</td>
<td>-50, -100, -150</td>
</tr>
<tr>
<td>Max</td>
<td>tdiff.spc</td>
<td>tdiff_txrx_max</td>
<td>temp</td>
<td>70, 120, 200</td>
</tr>
</tbody>
</table>

Parameterized subcircuit selection
Allowed values with 1st as default
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• Summary
Using AMI in conjunction with [External Model]

- Analog IO buffers in some cases could be modeled as s-parameters or as Spice sub-circuits. These models then work in conjunction with AMI code that represents DSP portion of IO-buffers. There could be even situations where IO-core itself becomes part of this AMI code.

- Hence we need to support AMI model simulation in absence of VI-VT data.
  - AMI model + Analog buffer represented as Spice-IO
  - AMI model + VI-VT Analog buffer + RDL (etc) in [External Model] (Case 1)
  - AMI model + Analog buffer represented as S-parameter-IO (Case 2)
  - AMI model (contains Analog-IO buffer coded as in AMI itself) + S-parameter/Spice RDL (Case 3)

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[External Model]
Language SPARAM
Type I/O

<table>
<thead>
<tr>
<th>corner</th>
<th>file_name</th>
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<tbody>
<tr>
<td>Typ</td>
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<tr>
<td>Min</td>
<td>io_min.s4p</td>
</tr>
<tr>
<td>Max</td>
<td>io_max.s4p</td>
</tr>
</tbody>
</table>

(VI-VT tables are not required as S-Params represent the analog I/O buffer or RDL etc + I/O buffer)

| Ports List of port names (in same order as in SPICE | SPARAM) |
| Ports A_signal_pos A_signal_neg my_receive my_drive my_enable |
| Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd |

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Using AMI in conjunction with [External Model]

Case 1

AMI + \[\text{[External Model]}\] + RDL(S-Param)

Case 2

AMI + [External Model] + I/O Buffer (S-Param)

Case 3

AMI Model + I/O Buffer + RDL(S-Param)
Summary

- Package parasitics can be modeled as SPICE using [External Model]; but we need to support S-parameters and it should be under proper keyword in Package-Section
- [External Model] has been traditionally used as alternate to VI-VT data; but we need to leverage it to use this model in conjunction with VI-VT
- [External Model] should support parameter switching to pick subcircuits dynamically
- AMI model today assumes analog-IO available as VI-VT; AMI model should work in conjunction with [External Model]