Model Connection Protocol
extensions for Mixed Signal SiP

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Agenda

- Why Model Connection Protocol
- Model Connection Protocol overview
- Extensions required for Mixed Signal SiP
- MCP Applications
- Summary
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design

- Design low impedance path: supply to chip
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design

Chip PDN models can vary from 2-node to N-nodes, where N is the number of physical pins.

There can be 1 to M current sources, where M may be much larger than N.
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design

- Chip/Package/Board have many physical connections
  - Chip-Package Boundary: 100-6000
  - Package-Board Boundary: 100-3000

- Not all electrical nodes can have per-pin resolution
  - Models may become too large for computation, simulation

- Need way to group pins and auto-connect models across IC/Pkg/Board
MCP Overview
- Establish mapping

Pin grouping and mapping

- physical pin (of layout) to electrical node (of model) per Net
- Mapping to connecting structure using physical location

Example of VDD net across chip-pkg-board

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**MCP Overview**

- Establish mapping

```
.subckt chip  d1 d2 d3 d4 d5 d6 d7
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] DIE
* [MCP Source] chip extraction tool
* [Coordinate Unit] um
* [Connection] pkg1 pkg_bumps 7
* [Connection Type] PKG
* [Power Nets]
  * pin1 d1 VDD 0 0
  * pin2 d2 VDD 0 100
  * pin3 d3 VDD 100 0
  * pin4 d4 VDD 100 100
  * pin5 d5 VDD 50 0
  * pin6 d6 VDD 50 50
  * pin7 d7 VDD 50 100
* [MCP End]
--- SPICE elements ---
.ends
```

```
.subckt package p1 p2 p3 p4
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] PKG
* [MCP Source] package extraction tool
* [Coordinate Unit] um
* [Connection] die1 myCPU 7
* [Connection Type] DIE
* [Power Nets]
  * 01 p1 VDD 0 0
  * 02 p1 VDD 0 100
  * 03 p1 VDD 100 0
  * 04 p1 VDD 100 100
  * 05 p2 VDD 50 0
  * 06 p2 VDD 50 50
  * 07 p2 VDD 50 100
* [Connection] board1 my_board 4
* [Connection Type] PCB
* [Power Nets]
  * 08 p3 VDD 0 0
  * 09 p3 VDD 0 200
  * 10 p4 VDD 200 0
  * 11 p4 VDD 200 200
* [MCP End]
--- SPICE elements ---
.ends
```

Example of VDD net across chip-pkg-board

**Pins of net**

**Electrical node**

**Netname**

**X-Y loc of pin**

```
.subckt board  b1
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] PCB
* [MCP Source] board extraction tool
* [Coordinate Unit] mm
* [Connection] pkg1 pkg_balls 4
* [Connection Type] PKG
* [Connection Type] PCB
* [Power Nets]
  * pin_1 b1 VDD 0.0 0.0
  * pin_2 b1 VDD 0.0 0.2
  * pin_3 b1 VDD 0.2 0.0
  * pin_4 b1 VDD 0.2 0.2
* [MCP End]
--- SPICE elements ---
.ends
```

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MCP Extensions for Mixed Signal SiP

- Analyze power-delivery to ICs when Package rails supply power to
  - different ICs that could be digital and/or analog
  - RF-modules and Passive/Active SMDs
- Need Schematic driven Mixed Signal Simulations to process IR-drop at power-rails

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MCP Extensions for Mixed Signal SiP
-Current MCP scope

Board -> Package -> DIE-Digital
MCP Extensions for Mixed Signal SiP

![Diagram showing the relationship between Board, Package, DIE-Analog, Module (Example RF module, SMDs), and DIE-Digital.]

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MCP Extensions for Mixed Signal SiP
- Mixed Signal IR-drop Task Flow

Schematic driven Analog

SiP & Circuit Design Schematic Capture

Pre- & Post-Layout Simulation

Analog IR-drop (schematic simulation driven)

Passive Structures

SiP Layout

Power-RAIL extract

Analog IC Layout

Power-Net Extract

Digital IR-drop

SiP

IC

MCP Physical

HDL

Digital IC layout

Power-Net Extract

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MCP Extensions for Mixed Signal SiP
- Electrical connectivity of models with disparate pin grouping

- Support for mapping of different electrical port-groups across different structures
  - As an example
    - a package model with 2-by-2 grid-based pin grouping
    - a chip model with 3-by-3 grid-based pin grouping
  - desired is an electrical circuit to interface between an 8 node circuit and an 18 node circuit
MCP Extensions for Mixed Signal SiP

- Optional Column for mapping of electrical nodes across structures

Package: .Subckt bp1 dp1

Board

bp1

DIE

Pin1 dp1 VDD 5 4 D1A
Pin2 dp1 VDD 6 4 D1A
Pin3 dp1 VDD 7 4 D1A
Pin4 dp1 VDD 8 4 D1B
Pin5 dp1 VDD 9 4 D1B

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Examine the nodes of each net

- for overlapping pin group domains, the corresponding nodes are shorted together:
  - (1,1) node shorts together {(1,1), (1,2), (2,1), (2,2)} nodes
  - (1,2) node shorts together {(1,2), (1,3), (2,2), (2,3)} nodes
  - (2,1) node shorts together {(2,1), (2,2), (3,1), (3,2)} nodes
  - (2,2) node shorts together {(2,2), (2,3), (3,2), (3,3)} nodes

  alternately
  - (2,2) node shorts together {(1,1), (1,2), (2,1), (2,2)} nodes

- all nodes are shorted together, reducing to per-net connectivity
  - instead of 8 or 18 node electrical connectivity it is actually 2 node connectivity

Recommendation

- Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains
  - but it can reduce the effective resolution of the model at the chip/package interface
  - Useful in case of early debugging and quick connectivity
Extensions over existing MCP
- Support for Modules as connect type structures

- Mixed Signal SiPs would have elements other than ICs like
  - RF modules
  - Metal Passive structures
  - SMD components
  - Silicon Interposers

- These structures draw power impacting PDN loading and hence we need to support [Module] category besides IC, Package and Board
Extensions over existing MCP

- Support for Modules as connect type structures

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Extensions over existing MCP
- Connection by Refdes besides X-Y location

- In order to connect to structures that are SMD or metal-passive structures on SiP – usually a case for Mixed Signal SiP, it becomes difficult to connect by X-Y locations.

- Early analysis may require quick way of stitching the models across structures and minor placement or resolution changes can cause X-Y mapping to fail.

- Optional column showing connection by REFDES makes easy mapping for Mixed-Signal modules and early trials

  - Examples of connecting interfaces could be
    - IO-cellname (DIE IO)
    - R1:1 (pin 1 of R1)
    - CONN:1 (pin1 of PCB connector)
    - my_model_opamp:3 (port-3 of opamp subcircuit)
Extensions over existing MCP
- Connection by Refdes besides X-Y location

- Simulating Analog DIE in package schematics with loading from passive structures connected to DIE
- The simulation data is post-processed to obtain IR-drop at power-rails

[connection type MODULE]

<table>
<thead>
<tr>
<th>Pin</th>
<th>dp</th>
<th>VDD</th>
<th>5</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin1</td>
<td>dp1</td>
<td>VDD</td>
<td>varistor1:2 //Reference_design:pin//</td>
<td></td>
</tr>
<tr>
<td>Pin2</td>
<td>dp1</td>
<td>VDD</td>
<td>varistor2:2</td>
<td></td>
</tr>
<tr>
<td>Pin3</td>
<td>dp1</td>
<td>VDD</td>
<td>7</td>
<td>4</td>
</tr>
</tbody>
</table>

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MCP applications: Digital DIE IR-drop
- Digital DIE in context of package model

Simulation results of Vdd rail: Dynamic IR-Drop

Without package effects
worst-case IR drop: 147.5mV

With package effects
worst-case IR drop: 179.3mV

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MCP applications: Analog DIE IR-drop
-Analog DIE in context of package model & Digital DIE-models

- Analog DIE test-bench with power-rail model
- Digital DIE model connected to represent loading of power-rail
- Analog DIE IR-drop post simulations
Summary: MCP format updated in context of Mixed Signal contents