Model Connectivity in PDN Analysis for 3D-SiP

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Outline

- 3D-SiP PDN analysis
- Interference issues in PDN
- PDN modeling strategy
- Model connectivity
- Case studies
PDN in 3D-SiP

Distributed dies
- Shared/isolated PG mesh on Silicon Interposer

Stacked dies
- Vertical PG paths by TSV
- Wirebond connections from package
Power Integrity Assessment

On-die decoupling effect

System operation
SSO impact

Frequency domain Characteristics

Time domain Noise analysis

Device parasitic

MOS cap

MIM cap

total $C_{pg} = 4\,\text{nF}$

$C_{pg} = 15\,\text{nF}$

$C_{pg} = 25\,\text{nF}$

Current excitation

Power rail collapse
Interference Issues in PDN

- Influence from adjacent circuits
- Die location dependency
- Coupling through Package

→ Simulation needs to efficiently reflect conjunctions between those “elements.”
Influence from Adjacent Circuits

\[ \Delta V_i = I_i \times Z_{ii} + \sum_{j \neq i} I_j \times Z_{ij} \]

Input Impedance

\[ Z_{ij} = \frac{V_i}{I_i} \]

Transfer Impedance

\[ \sum_j Z_{ij} = \sum_j \frac{V_i}{I_j} \]
Die Location Dependency

Transfer Impedance: $Z_{BA} < Z_{DC}$

3D-SiP structure trade-off

→ Wide IO band width with less power consumption
→ Tighter interaction between dies in a localized PDN
**Coupling through Package**

- **Chip/interposer PDN** → Highly resistive, high loss

- **Package PDN**

**High loss chip PDN**
- Power rail noise is spread out thru package.
- Effective area of on-chip decap is limited.
System-level Co-simulation Workflow

1. Noise Source Generation
   - Current Signature Synthesis
   - TWF
   - DEF
   - .lib
   - SPEF
   - VCD

2. Chip Model Generation
   - GDS
   - PDN Extraction
   - .subckt Chip A
   - .subckt Chip B
   - .subckt Interposer

3. Package/Board Model Generation
   - Package/Board design
   - PDN Extraction
   - .subckt Pkg & Bd

4. Model Organization
   - Combine Circuits
   - Top level 3D-SiP Model

5. Simulation
   - TD Analysis
   - FD Analysis

- Circuit block PWL
- Cell Cpg
- Package/Board design
- PDN Extraction
- Top level 3D-SiP Model
- TD Analysis
- FD Analysis
PDN Modeling Strategy

- Model resolution
- Chip-centric observation
- Model connectivity
Model Resolution

Pin location resolution

- Power/ground pin characteristics are sensitive to the structure.

Circuit (cell/block) placement resolution

- Simulation priority
  - accuracy with detailed placement
  - faster run time with rough floor plan
Chip-centric Observation

- Nodes/Ports on the device layer are necessary as well as bump/pad layer.
Model Connectivity

- The model connection scheme affects simulation resolution and accuracy.
- Per-pin connection is important in order to predict localized propagation/distribution of PDN behavior of 3D-SiP.

Example: Automated pin matching (> 5,000 power/ground pins) for wrapped circuit generation.
Unified Protocol for Model Connections

In order to achieve ...

- Automation in simulation setup.
  ⇒ ease of use, reduction of engineering time.

- Mixed simulation environment.
  ⇒ various model resources and methodology.
Example of Proposed MCP™ (Model Connection Protocol)

```
.subckt package p1 p2 p3 g1 g2 g3 s1 s2
  * [MCP Begin]
  * [MCP Ver] 1.1
  * [Structure Type] PKG
  * [MCP Source] package extraction tool
  * [Coordinate Unit] um
* [Connection] chip U1 5
  * [Connection Type] DIE
  * [Power Nets]
    * A1 p1 VDD 0 0
    * C3 p2 VDD 200 200
  * [Ground Nets]
    * A3 g1 VSS 0 200
    * C1 g2 VSS 200 0
  * [Signal Nets]
    * B2 s1 IO1 100 100
* [Connection] board U2 3
  * [Connection Type] PCB
  * [Power Nets]
    * a1 p3 VDD 0 0
    * c3 p3 VDD 1000 1000
  * [Ground Nets]
    * a3 g3 VSS 0 1000
    * c1 g3 VSS 1000 0
  * [Signal Nets]
    * b2 s2 IO1 500 500
* [MCP End]
  --- SPICE contents ---
.ends
```
Connection Density Control

- The difference of node resolution between the models can be handled in MCP™.
- But it is desired that a model have the same pin resolution as the destination circuit.
Previous Discussions

- “Model Connection Protocols for Chip-Package-Board System-level Analysis”
  Sigrity, Inc.
  IBIS Summit, DAC / July.28, 2009

- “An Introduction to Model Connection Protocols”
  Sigrity, Inc.
  IBIS Summit, DesignCon / Feb. 4, 2010

- “Model Connection Protocol extensions for Mixed Signal SiP”
  Cadence Design Systems, Inc.
  IBIS Summit, Tokyo / Nov. 15, 2010
3D-SiP Case Studies: Location dependency

Port location in Chip-A/C layout (top view)

- Port1-1
- Port2-1
- Port3-1
- Port4-1
- Port5-1
- Port6-1
- Port7-1
- Port8-1

- Port1-2
- Port2-2
- Port3-2
- Port4-2
- Port5-2
- Port6-2
- Port7-2
- Port8-2

1,500 pins connection for one power net

Input Impedance

Z Amplitude (Ohm)

Frequency (GHz)

Chip-A

Chip-C
Virtual model connections for what-if analysis can be easily performed by MCP™ utilization.
Thank You!