Board-only Power Deliver Prediction for Voltage regulator and Mother Board Designs

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Agenda

• Introduction
• Simplified SPICE Model
• Case Study and Its Application
• Validation
• Summary and Next Steps
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Introduction

Power delivery performance prediction typically is using full wave solvers to extract board, socket, package, and on-chip interconnect. There are many tools and approaches across industries.

However, this typical approach is usually focusing on high frequency noise, involving many piece of software and has certain limitations:

• Very high frequency oriented analysis. Typically looking for many 100s MHz or GHz range
• Extracted full wave S parameters needs macro-modeling for transient analysis
• All full wave solvers has accuracy limitation at low frequency and board analysis needs very accurate low frequency prediction
• Full wave extraction and its associated analysis do not have full explicit information on return path (GND) which is critically important for board design and optimizations.
• Typically full wave approach takes much more time to complete an analysis cycle and also needs electro-magnetics background for many uncertain scenarios during modeling/sims
• Due to its complexity, some OEM/ODM skip prediction step and go directly for testing vehicles
• Therefore, a method that involves less steps, easy to understand, good low frequency accuracy and high efficiency is highly desired!
Introduction (cont’d)

A new methodology is called ‘Simplified SPICE Model’. It allows companies to conduct simulations focused on the follows:

- Determine # of MB layers and stack-up
- Choose MB cap types, numbers and locations
- Check the coupling noise due to imperfect common ground
- Validate MB and VR performance in early development stage
- Reduce design cycle time due to faster simulations
- A lot more accurate at low frequency regions.
- Explicitly know exactly return currents
- Least software involvement
- An entry engineer can conduct modeling/simulations
Agenda

- Introduction
- ✔ Simplified SPICE Model
- Case Study and Its Application
- Validation
- Summary and Next Steps
A Typical Network for MB Power Delivery Analysis

MB R network start from VR output Buck Cap

Use Icc / Isa / Itt current Models to replace Die+package models and represent VRTT

MB R network end at Socket pins

Conventional PD Models:
Die (on-die caps) + Package(with caps) + socket + MB + MB/Bulk caps + VR

Simplified SPICE Model for OEMs/ODMs:
VRTT (Icc/Isa/Itt) + socket + MB + MB/Bulk Caps + VR
Simplified SPICE Model Workflow

Step 1. Create MB model
- Create R-network using EDA tool.
- Set up port locations for cap terminations and Vcore, Vsa, Vtt, and socket locations.

Step 2. Socket model
- Get socket pin map from supplier.
- Get R & L values of each socket pin from supplier.
- Group socket pins and scale R & L values.

Step 3. Icc, Isa, Itt models
- Get I (t) model from supplier

Step 4. VR model
- Use simple VR model from supplier.

Step 5. Connect all models together and run transient simulations
- Vcore(t), Vsa(t), Vtt(t) separately

Step 6. Compare V(t) with DC and Transient Requirements
For VR design: we’ll provide current models of Vcore, Vsa, and Vtt and indicate the locations of the socket pins to connect your MB. MB models will only include R from Power/Ground planes and vias.
I(t) Models of Vcc/Vsa/Vtt

A server CPU
150 W PVCCP (8 core)

Max step load size = 100 A
Max step load slew rate \( \frac{di}{dt} \leq 200 \text{ A/}\mu\text{s} \)

A server CPU PVSA

Max step load size = 7 A (Current pulse duration <1\( \mu \text{s} \))
Max step load slew rate \( \frac{di}{dt} \leq 4.0 \text{ A/}\mu\text{s} \)

A server CPU PVTT

Max step load size = 5 A
Max step load slew rate \( \frac{di}{dt} = 20 \text{ A/}\mu\text{s} \)
## Socket Connections (Top MB Layer, 1 of 5)

<table>
<thead>
<tr>
<th>MB nodes</th>
<th>PKG nodes</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>VCCU pins</td>
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<tr>
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<td>bx11y21</td>
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<tr>
<td>Y33</td>
<td>bx11y22</td>
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<tr>
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<tr>
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</table>

You may need to lump several pins as one node.
## Stackup (6 layer)

<table>
<thead>
<tr>
<th>Layer Name</th>
<th>Plane Description</th>
<th>Layer Thickness (mil)</th>
<th>Copper Weight (oz)</th>
<th>Dielectric (eR)</th>
<th>tand (max)</th>
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<td>4.0</td>
<td>0.022</td>
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<td>Plane 2</td>
<td>GND</td>
<td>1.30</td>
<td>1.0</td>
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<tr>
<td></td>
<td>Prepreg</td>
<td>4.00</td>
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<td>4.1</td>
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<tr>
<td></td>
<td>core</td>
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<td>1.0</td>
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<td></td>
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<tr>
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<td>Prepreg</td>
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<td>4.1</td>
<td>0.022</td>
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<tr>
<td></td>
<td>prepreg and/or Core</td>
<td>2.70</td>
<td></td>
<td>4.0</td>
<td>0.022</td>
</tr>
<tr>
<td>Signal 6</td>
<td>SIGNAL</td>
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<td>1.5</td>
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<tr>
<td></td>
<td>solder mask</td>
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<td></td>
<td>3.8</td>
<td>0.022</td>
</tr>
</tbody>
</table>

Total 62.40 (+8/-5)

You may want to get MB resistivity value from MB suppliers.
Simplified SPICE Model

Simplified Multiphase VRD (P1~P4) with Socket LoadLine

Simplified MB R network include Bulk Caps & Decoupling HF Caps

Icc / Isa / Itt current SPICE Model

Sensing at CPU Socket
SPICE Model Connection Block Diagram

- **Socket Model**
- **Icc Model**
- **VR Model**
- **MB R network Model**
- **Bulk Caps**
- **HF Caps**

- **P1**
- **P2**
- **P3**
- **P4**
- **Vsense +**
- **Vsense -**
- **GND**
- **MB SKT +**
- **MB SKT G**
- **Cap +**
- **Cap G**

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DC Requirements

Socket Load Line

Vccmax Violation

Operation in this region may result in reduced life span due to processor/system heat damage. Also system speed degrades due to repeated transitions into low power state to cool processor.
DC Requirements (cont’d)

Operation in this region may result in system ‘lock-up’, system ‘blue-screen’, or corrupt data.

Vccmin Violation
Dynamic or Transient Requirements

Short transients above VID are permitted see the overshoot specification

Load step to Icc max
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Cost/Performance Optimization study of Cap number:

- **Case 1** ~ 10 μF 50 pcs / 22 μF 16 pcs / 470 μF 7 pcs
- **Case 2** ~ 10 μF 30 pcs / 22 μF 8 pcs / 470 μF 4 pcs

### Top caps
- 25-10 μF
- 8-22 μF
- 2-470 μF bulk caps

### Bottom caps
- 25-10 μF
- 8-22 μF
- 5-470 μF bulk caps
Case Study – Cost/Performance Optimization of Cap number

If transient design target is A, both Cases 1 and 2 fail.
If transient design target is B, Case 1 is fine but Case 2 fail.
If transient design target is C, both Cases 1 and 2 are fine.
Agenda

- Introduction
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- Case Study and Its Application

✓ Validation

• Summary & Next Steps
Simulation Result vs. VRTT Test Result

Loading frequency = 305 Hz
Slew = 163 A/μS

1st spike reading:
1.058 V vs. 1.05 V @ 115 A to 25 A 8 mV difference only → 99.24% Accuracy

• Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
• Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.
Simulation Result vs. VRTT Test Result

Loading frequency = 305 Hz

Slew=163 A/μS

1st spike reading:

0.914 V vs. 0.932 V @ 25 A to 115 A  **18 mV** difference only → **98.07% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.
XYZ CRB Simulation Result vs. VRTT Test Result

Loading frequency = 12K
Slew=163A/μS

1st spike reading:

1.052 V vs. 1.054 V @ 115 A to 25 A  2 mV difference only → 99.8% Accuracy

0.914 V vs. 0.934 V @ 25 A to 115 A  20 mV difference only → 97.85% Accuracy

• Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
• Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.
Simulation Result vs. VRTT Test Result

Loading frequency = 275K
Slew=163 A/μS

1st spike reading:

1.064 V vs. 1.066 V @ 115 A to 25 A  **2 mV** difference only → **99.8% Accuracy**

0.914 V vs. 0.94 V @ 25 A to 115 A  **26 mV** difference only → **97.63% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform ∆.
- Adding MB parasitic C & L should be helpful in reduction of waveform ∆ as well.
XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 650K
Slew=163 A/μS

1st spike reading:
1.034 V vs. 1.048 V @ 115 A to 25 A  **14 mV** difference only → **98.66% Accuracy**
0.92 V vs. 0.93 V @ 25 A to 115 A  **10 mV** difference only → **98.9% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.
Simulation Result vs. Real VRTT Test Result

1st spike reading:
1.15 V vs. 1.143 V @ 165 A to 59 A  7 mV difference only
1.09 V vs. 1.095 V @ 59 A to 165 A  5 mV difference only

Simulation Result Accuracy higher then 99%
* (This case used a very sophisticated VR model from VR Vender.)
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- Introduction
- Simplified SPICE Model
- Case Study & Its Application
- Methodology Validation

✓ Summary and Next Steps
Summary and Next Steps

Simplified SPICE model has been validated by companies

Using the collaterals, companies can

- optimize their own designs & make their own decisions before Gerber Out to achieve the best cost/performance trade-off in
  - Determine # of MB layers & stack-up
  - Choose MB cap types, numbers & locations
- reduce risk of common ground noise coupling among Vcc, Vsa, Vtt, and Vddq
- validate their own designs after Gerber Out

Next Steps

- Obtain more sophisticated VR model from vendors
- Include thermal impact to more accurately predict Maximum Current can be carried.