Power Aware Features of IBISv5.0 – Accuracy and Challenges

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Asian IBIS Summit
Taipei, Taiwan
November 21, 2011
Agenda

- Introduction
- BIRD98 [ISSO PU] / [ISSO PD]
- BIRD95 [Composite Current]
- Accuracy Enhancements
- Challenges
Introduction

- For Improved SSO simulations in non-ideal power supply environment IBIS ver.5.0 introduced the following features:
  
    - To model Gate Modulation effect.

  - Added [Composite Current] tables proposed in BIRD95.
    - For more accurate analysis for ground and power bounce associated with simultaneous switching noise.
Due to SSO noise, the actual drive strength may vary during transients depending on the instantaneous value of the supply voltage.

- This phenomena is usually called the "Gate Modulation Effect"

- In IBIS (prior to IBISv5) Working point can move only along the same $V_{gs} = V_{DD}$ characteristic.

- During supply bounce, actual working point shifts to $V_{gs} = V_{DD} \pm \Delta V_{bounce}$ characteristics.

- Higher is the bouncing noise, the higher is the mismatching between IBIS and Spice results.

- [ISSO PU] / [ISSO PD] define the effective current of the pullup/pulldown structures as a function of the voltage on the pullup/pulldown reference nodes.
The current causing the Supply bounce will include:

- \( I_{\text{byp}} \) - Bypass current
- \( I_{\text{pre}} \) - Pre-Driver current
- \( I_{\text{cb}} \) - Crow-bar current
- \( I_{\text{term}} \) - Termination current (if Present)

\( I_{\text{total}} = \) \( I_{\text{byp}} + I_{\text{pre}} + I_{\text{cb}} + I_{\text{term}} \) ([Composite Current])

- \( I_{\text{byp}} \) & \( I_{\text{pre}} \) play a significant role in determining the supply bounce.
- Not modeled by IBIS ver. Prior to 5.0

Describes **Rising** and **Falling** edge total current from the **Power Reference** terminal of the buffer.

*Image taken from IBIS 5.0 Specification document.*
“The currents documented in the I-T table correspond to the voltages in the V-T table at the identical time points and for the given *fixture load.” *

- The best data points for a specific V-T table will not be the same best points for corresponding I-T table.

- Generation tools can miss important information in I-T data.

*Text taken from IBIS 5.0 Specification document.*
For High Speed buffers, Some simulators require removal of Initial dead time (if greater than half bit period of the driving signal), to avoid overclocking.

- If Initial dead time removed from V-T tables, I-T waveforms also need to be adjusted similarly.
- Pre-driver current information will be lost.
- [Composite Current] information cannot be effectively used.
- Model developers need to support 2 Separate Models, one with dead time removed and other without removal.

This constraint (I-T data time-correlated with V-T data) need to be removed to accurately model the V-T Waveforms and I-T waveform. ("BIRD 141")
[Composite Current] Observation 3

- No info regarding Pull Down reference terminal current in IBIS models !!
  
  - Simulators can only assume Pull Down terminal current equal to Pull Up reference current ?
  
  - Accuracy of Power Down terminal current simulations reduced.
  
  - May impact SSN number estimation.
Accuracy Enhancements
Comparison of power/ground supply node current and voltage for IBIS 4.2 and IBIS 5.0 model with Reference Spice model in SSO simulation.

- Corner: Max.
- Frequency: 50MHz
- Far End Capacitive Load: 25pF
- Decoupling Capacitance between Supply and ground of each Buffer: 4pF
Result 1: I(VDD)/V(GND) SPICE-IBISv4.2-IBISv5.0

- Improved matching in Power supply current simulation.
- Improved matching in Supply bounce simulation.

Accuracy Enhanced of IBIS Models With:

[Composite Current], [ISSO PU], [ISSO PD].

* From SPICE simulation
Result 2: I(VDD)/V(GND) SPICE-IBISv5.0 (with & without decoupling capacitance)

- Improved matching with de-cap added to spice model in **Power supply current** Simulation.

- Improved matching with de-cap added to spice model in **Ground bounce** Simulation.

No method to specify ‘individual buffers internal De-coupling capacitance’ between its supply nodes in IBIS syntax.

* From SPICE simulation
Challenges

- **[Composite Current]** time-correlation with V-T waveforms can lead to loss of important pre-driver current info in overclocking and non-overclocking models. This constraint need to be removed.

- No method to specify ‘**individual buffers internal De-coupling capacitance**’ between its supply nodes in IBIS syntax
  
  - Can specify On-die decoupling capacitance between pins using Series Model at component level.
  
  - As a model supplier, Internal de-coupling capacitance is required during validations as well as to pass on this info to customers for simulations at their end.
THANK YOU