Designing DDR3 system using Static Timing Analysis in conjunction with IBIS simulations

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Agenda

- Key Design Challenges
  - DDR3 Timing and SI specifications

- Problem Statement
  - Piecemeal simulations do not guarantee optimal design

- Solution
  - Static Timing Analysis in conjunction with IBIS simulations

- Use-cases
  - Step-by-step method to optimally use EDA flows

- Summary
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Key Design Challenges

Timing Budget

Signal Quality

Component selection

Stack-up and Layout

DDR3
Board design
Large solution space
To be explored
Key Design Challenges: Timing Budget

- **Set-up / Hold Times**
  - Data write w.r.t strobe
  - Data read w.r.t strobe
  - Addressing w.r.t clock

- **Strobe w.r.t clock**
  - Data w.r.t Address

- **Account for**
  - Clock/Strobe Jitters and Interconnect Jitters
  - Slew-rates and hence derating of setup/hold
Key Design Challenges: Signal Quality

• Thresholds
  – DC and AC
  – Noise-Margins
• Overshoots/Undershoots
  – Magnitude
  – Area
• tVac
  – Minimum time for signal to stay above threshold
• Eye
  – Data-Valid Window after accounting Jitter
• Slews that in-turn affect timing
  – Rise/Fall times
Key Design Challenges: Component Selection

- Memory-Buffers
  - Trade-off between read-write cycles
- Controller Driver strength
  - Trade-off between read-write cycles
- Connector
  - Insertion loss
- Strobe/Clock differential buffers
  - Should satisfy tDVac and overshoot/undershoot area requirements
Key Design Challenges: Layout Constraints

• Trace-lengths
  – Relational Propagation-delays Data-Strobe for balanced setup/hold
  – Relational Propagation-delays Address-Clock for balance setup/hold
  – Relational Propagation-delays Strobe-Clock for successful write-leveling

• Topology schedules
  – Point to Point for Data
  – FlyBy for Address

• Trace Impedance
  – Example: Lead-in section (45 ohm) to Load-in section (60 ohm) through neck-down (~5 to 10 mm) for clock
  – Percentage variation that can be tolerated

• Differential matching (CLK, STROBE)
  – Maximum unparallel length
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Problem Statement: Multiple constraints across Timing / SI

• DDR3 has several SI and Timing constraints and getting all of them to meet is a big solution-space to explore.

• Designer tries to fix a few; and in the process puts other measurements-of-interest out of specifications.
Problem Statement: Timing Closure across read/write/address

- Timing-Closure is time-consuming as there are too many constraints to be met
  - Etch delays needed for timing-closure during Read cycle may not work during Write cycle.
  - It is not enough to get just positive Setup/Hold margins; optimal design needs setup and hold margins that equally distributed.
- Requirement of relative delays between Data (Strobe) vs Address (Clock) brings additional challenge.
- It is also important to budget for signal and interconnect jitters on various signals.
  - What may look to be meeting the constraint is likely to fail due to jitter causing uncertainty in the signal.
Problem Statement: SI affects timing

• Slew-rates affect Setup/Hold time-constraints.
  – SI simulations provide slew-rates of signals that in-turn need to be considered for timing constraints. For example, hold-time constraint could be 160pS for slew-rate of 1V/ns while it could be 200pS when the signal slew-rate is 2V/ns

• Eye-shape could indicate a need for different relative etch-lengths for equal setup/hold margins.
  – While Static Timing Calculations would provide one set of readings for etch-delays, the eye-shape (that could be narrow on one side) may force the designer to refine the relative delays for balanced setup/hold times.

• Stack-up variation and Cross-talk causes interconnect jitter that needs to be accounted for in the timing-checks.
  – It is important that such jitter is estimated through SI simulations and then annotated to the Timing-models for timing closure.
Problem Statement (Current approach): Ad-hoc analysis and verification (Leading to Non-optimal design)

- Timing-checks are done using hand-calculations at times and then the focus is to do post-layout verification using SI simulations to ensure correctness.

- Limitations:
  - Goal is to just meet constraints as against optimal design with enough margins on all constraints.
  - Manual timing-budget calculations are time-consuming and inefficient
  - No way to include SI effects into timing-calculations
Problem Statement (Current approach) : Ad-hoc analysis and verification (Leading to Non-optimal design)

- Designers use layout rules provided by device manufacturers
- Limitation:
  - Limits flexibility. PCB designers refrain from trying variations in terms of component selection from different vendors and in trying different board dimensions and circuit configurations.
  - Over-design at times as layout guidelines are usually on the stricter side to ensure working of system
Problem Statement (Current approach)
: Ad-hoc analysis and verification (Leading to Non-optimal design)

- SI simulations are usually done as audit at verification step following a piecemeal approach
- Limitations:
  - Use of real-time simulations to do exhaustive timing-verification is too time-consuming and difficult.
  - It is very difficult to manage optimal parameter selection across constraints spread across read/write and address cycles.
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Unified SI/STA flow for DDR3

Etch-delay estimation for timing

Signal-Integrity checks using estimated etch-delays

Etch-length and Buffer strength (ODT) refinement for better eye

Pre-layout Signal-Integrity to Timing-closure

Generation of layout constraints for board routing based on SI topologies

Post-layout Bus simulations and Timing closure
Solution: Static Timing analysis

- Static Timing exploration independent of time-expensive SI simulations can provide seed for etch estimation.

- Automatic update of constraint limits based on data-rate, slew-rate of signals, threshold-values selected for design can make easy computation.

- Automatic calculation of relative etch-delays for balanced setup/hold times while accounting for uncertainty in signals due to jitter can save multiple iterations.
Solution: Timing analysis feeds SI simulations

- Results of STA feed into SI simulations.
  - Estimated etch-delays (flight-time) of data, strobe, address, clock map to interconnect flight-times
  - Estimated jitter becomes constraint for cross-talk (interconnect and data-dependent)

- SI Simulations with IBIS buffers
  - Building on interconnect details (vias, trace-lengths, stack-up) keeping the flight-time constraint from STA
  - Improving on interconnect topologies to meet SI constraints and better centering of strobe w.r.t data
Solution: SI simulations that feedback STA

- Feed-back updated flight-times (switch-delays), worst-jitter and slew-rates from real-time SI simulations to timing-models to close timing-constraints.

- Generation of layout constraints from interconnect topologies
  - Routing the board based on layout constraints

- Post-route SI simulations followed by timing-closure.
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Use-case

Controller Model

Timing/Deration Model

Connector Model

Memory Model

Electrical Constraints

DIMM topology / boards
Building Project

- Frequency of operation and AC threshold levels
  - Configures TD models
  - Configures custom measurements
- Address (1T / 2T)
  - Configures TD models
- New DIMMs (Or On-board) vs Existing DIMMs
  - Pre-created Topologies vs Extracted DIMM topologies
- DIMM Card Type
  - Configures topologies and ECSets
Timing estimation

- **Data-Strobe**
  - Write
  - Read
- **Address-Clock**
  (1T or 2T)
- **Decide etch-delays that can meet timing specifications**
**IO-model selection/Exploration**

- For best noise-margins and Eye for read/write

- Controller Model
  - Impedance

- Memory Model
  - ODT

- Connector Model

- Strobe
  - $tv_{ac}$, shoot-area
SI Solution Space for Relational Topologies - Explore data w.r.t strobe; address w.r.t clock
Timing Verification after SI-annotation

- Re-verify timing after import of flight delays and jitter from SI simulations
Setting up Layout constraints depending on SI exploration

- Propagation Delays
- Impedance
- Relative Propagation delays
- Max Parallel
Post-layout verification and Timing closure
Use-Case: Reverse-engineer a board

Pick DDR3 board
Designed at 800Mbps

Extract topology

SI verification and exploration For 1333 Mbps

Timing Closure against
1333 Mbps data-rate
Timing model

ECset generation

Bus-Analysis on
Updated board

cadence
Use-Case: Correcting IC-PHY given board

- DDR3 reference board
- Extract routed nets and Do SI simulations
  - Find Propagation delays
  - Estimate jitter that can be tolerated for given DDR measurements
- Timing Exploration for Buffer
  - TCO delays
  - Write-leveling delays
  - PLL jitter / DCD
- SI verification using SPICE IO-buffer models
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- DDR3 compliance requires multiple specifications to be met, covering timing and signal-integrity measurements.
- Just using SI simulations to meet all specifications and explore solution space is difficult.
- Use of tools in a piecemeal approach can validate specifications but may not result in the most optimal IC/package/board design.
Summary

• Use of STA in conjunction with SI simulations in a methodical manner is needed to achieve optimal design.
• Timing models should be able to handshake data with IBIS simulations at pre-route exploration and post-route verification stages to ensure that both SI and Timing constraints are met.