The Evolution of DDR Memory and Overcoming Challenges of DDR3/4 Design

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Shanghai, China
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SI Product Manager
JEDEC recently announced the DDR4 standard
- September 25th, 2012
- JESD79-4

Major Implications:
- Point to Point Architecture
  - x4, x8, and x16 supported
  - 2GB to 16 GB SDRAMs
  - 1.2 V system
    - Vrefdq – on die reference voltage for DDR4
    - Up to 40% reduction in power
    - Pseudo Open Drain Silicon architecture vs. push/pull
      - Pulled to Vdd thereby only drive low to zero
- Data bus inversion
  - Limits # of SSO at a single time to improve SI and reduce power
- Write leveling for CMD/ADD, CNTL and CLKs to control skew due to Fly-by topology
- Server design
  - Distributed buffers for each byte lane compared to single buffer for all 64 bits
  - Point to Point topology requiring a switch between DIMMs
- Support for Chip Stacking
  - TSV Supported architectures for SDRAMs
T-topology vs. Fly-by topology

**DDR2 T-topology**

Clock arriving time to all DRAMS on a DIMM are expected to be the same

**DDR3 Fly-by topology**

Clock arriving time to each DRAM on a DIMM are different
Point to Point vs. Multi-Drop

**Multi-Drop Bus**
- DDR3 Memory Controller
  - DIMM
  - DIMM
  - DIMM
  - DIMM

**Memory Channel**

**Point-to-Point**
- DDR4 Memory Controller
  - DIMM
  - DIMM
  - DIMM
  - DIMM

**Memory Channel**
Server Architecture with Switches
DDR 3 Key Spec

Setup Margin & Hold Margin

Setup Margin

Hold Margin

Jitter
DDRX Technology & Challenges

• Design challenges?
  – Validation
    • Prototype
    • Measurement
    • Interpret and implementation (calculation) of Design Spec such as DDR3/4, LPDDR2/3 and more...
    • Large amount output data report of results
  – Capacity or Complexity and Time
    • Chip to Chip or Chip to PKG
    • Chip + Package + PCB + Connector/Cable + PCB + Package + Chip
    • Full System

227 pages of DDR3 spec
214 pages of DDR4 spec
199 pages of IBIS v5.1 spec
1. Higher Speeds
   - 66 Mbps to 3200 Mbps and beyond
   - Higher speed and edge rates cause more problems with skew, coupling, radiation, etc...
   - Timing margins become tighter; Setup and Hold timings
     - DDR 400 has a window of 2.5 ps
     - DDR4 3200 has a window of 312.5 ps

2. Changes with design topology
   - DDR2 started ODT support
   - DDR3 started Fly by topology vs. T topology
   - DDR3 uses only differential strobes
   - DDR4 architecture is point to point
     - One controller to 1 DIMM
   - DDR4 is Psuedo Open Drain vs. Push/Pull
## DDRX Technology Challenges

### DDR3 Compliance Report

#### Design Summary
- **Project**: bytes_bank_0912_test
- **Design**: GDT_40
- **Design ID**: 141
- **Design Type**: Circuit Design
- **Location**: F:\WORK_2012\09_DDR3 Tool Kit\New UDO_40_3_3
- **Date**: 9/28/2012 11:01 AM
- **Product Version**: Designer 6.0
- **UDO Version**: DDR3 Compliance Report, 1.0 (R.14.3)
- **User**: eonyong

#### Solution Setup

### Solution Details

#### Description
- **Name**: DDR3 AC-Timing S-DQ1
- **UDO**: C:\Program Files\ANSYS Designs\0\Windows\yzyd\UseDefinitions

#### Parameters
- **AC DQ Level**: AC150
- **Speed Bin**: Auto (from DQ)
- **DQ delay**: 0ps
- **External Report**: off

#### Per-Lane

### AC Timing (JESD79-3E, Section 13.1)

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<th>Metric</th>
<th>Worst Actual</th>
<th>Worst Margin</th>
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### Per-DQ

#### TVb(base) - Timing Metrics

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#### TVd(base) - Timing Metrics

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DDR3 Connector Impact (Reflections)

Without Connector

With Connector
DDR3 1.5V PDN with VRM
DDR3 1.5V PDN with VRM

~ 3-4 mV Drop
System Level Memory Analysis

SSO on Power Nets

F0_A0 BUS
System Level Memory Analysis

SSO on 12V Power Nets

SSO on 1.5V Power Nets
System Level Memory Analysis

SSO on 12V Power Nets

SSO on 1.5V Power Nets
Recall Chip Impedance

Package Layout

CPM

Vdd

Vss

Zin

Solder Bumps

Solder Balls

Vdd

Short

Vss

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Impedance Results with & without Chip

Red = Chip + PKG
Green = PKG
Die Solder Bump Voltage
Conclusion

• DDR4 Standard was recently released
  – Interconnect challenges due to Chip, PKG, & PCB
    • Reduced Voltage (1.2V -> 1.05V expected)
    • Increased Data Rates (1600 Mbps -> 4266 Mbps expected)
    • Future stacking of SDRAMs expected with TSV technology

• System level performance must include:
  – Accurate PKG/PCB extractions including connectors
  – Accurate Die Models: IBIS + current?