The Application of Simulation Kit Using USB3.0 IBIS-AMI Model

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Outline

- USB3.0 Compliance Simulation using IBIS-AMI Model

- Summary

- Expectation of IBIS-AMI
Outline

■ USB3.0 Compliance Simulation using IBIS-AMI Model

■ Summary

■ Expectation of IBIS-AMI
Chip-PKG-PCB Co-Design of SerDes I/F

- 5Gbps SerDes I/F become prevalent, for example USB3.0.
- We want to bring a new product to market more quickly.

Performance is improved.
How we balance TAT with cost?

In addition to performance, TAT and cost are important.

Performance is important.

In this presentation, I will focus attention on USB3.0.

Time to market
Product cycle is short
[Conclusion] : Only 0.5h for USB3.0 Analysis

- Measurement vs Simulation

IBIS-AMI enables a high accuracy and short TAT analysis.

Simulation is possible many times at the initial designing stage.

Spice Net Transient Analysis
Simulation time: 1Mbit(Conversion), 120,000h

IBIS-AMI Channel Analysis
Simulation time: 1Mbit, 0.5h

1000Bit 12h
1/240,000

match
match
USB3.0 Compliance Test Simulation Kit

USB3.0 Compliance Test Simulation Kit on EDA Tool

**Semiconductor Vendor**

1. Simulation Kit that reflected reference design.
2. Customer can judge the quality of own design quantitatively.
3. Customer can execute differential analysis in a short TAT. (IBIS-AMI + EDA tool)

**Customer**

4. The support of customer's difference analysis is easy.
5. EDA tool support.

**EDA Vendor**

Simulation Kit can prevent the troubles, for example mismatch between IBIS-AMI and EDA tool, the usage of EDA tool.
Contents of Simulation Kit

Simulation Kit

Reference Design

Stimulus

Bit Pattern

IBIS-AMI

Tx Model

S-Para

PKG Model

S-Para

PCB Artwork

PCB Guide

Ball Assign

Simulation Deck

Connector

R1

1.0 milliohms

R2

1.0 milliohms

Sim Result

Eye Mask

Rx Model

IBIS-AMI

Cable + Back Panel

Reference Cable(3m)

Reference Back Panel

RX(w/ CTLE)
Compliance Test Pattern (Stimulus)

USB3.0 Tx Compliance Test Pattern & Transmitter Eye

“Universal Serial Bus 3.0 Specification Revision 1.0”

Table 6-7. Compliance Pattern Sequences

<table>
<thead>
<tr>
<th>Compliance Pattern</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP0</td>
<td>D0.0</td>
<td>scrambled</td>
</tr>
<tr>
<td>CP1</td>
<td>D10.2</td>
<td>Nyquist frequency</td>
</tr>
</tbody>
</table>

CP0 : 8B/10B pattern (PRBS is encoded)

Eye Height, Jitter(10^{-12}BER) Measurement

$CP0 \times 10^6 \text{ UI} + CP1 \times 10^6 \text{ UI}$

Simulation time is too long in Spice Net Transient Analysis

about 5000 days!

Channel Analysis using IBIS-AMI

about 0.5 hours!
Channel Analysis

1. Analog Channel Impulse Response Process

2. Convolution Process

We can execute the analysis of 1 million bits in 0.5 hours.
Characteristic of IBIS-AMI

IBIS-AMI

IBIS-AMI: Algorithmic Modeling Interface

User can not correct IBIS-AMI, because AMI parts are black box.

Model maker should verify the quality of own IBIS-AMI. (each OS, EDA tool)

[Algorithmic Model]

IBIS Example

Executable Windows_VisualC_32 TX_Wx32.dll TX.ami
Executable Windows_VisualC_64 TX_Wx64.dll TX.ami
Executable Linux_gcc4.4.2_32 TX_Lx32.so TX.ami
Executable Linux_gcc4.4.2_64 TX_Lx64.so TX.ami

[End Algorithmic Model]
Trouble Case of IBIS-AMI Analysis (1/2)

Model dependence

CTLE characteristic (Reference Equalizer)
CTLE: Continuous Time Linear Equalizer

Some EDA tools are OK. Others are NG.

All EDA tools are OK.
Trouble Case of IBIS-AMI Analysis (2/2)

- **Tool dependence**
  - Samples Per Bit Interval
    - => Default Setting

  Voltage level is out of order!

- **Samples Per Bit Interval**
  - => Recommended setting

  The setting value depends on modeling of IBIS-AMI. It is necessary to use the recommended value.

It is important that IBIS-AMI model maker solve various problems of “model and tool dependence”, before model maker release it.
Reference Design (Differential Analysis)

At the environment building

- **Ball Assign**
- **PCB Guide**
- **PCB Artwork**

Tx/Rx Model

- **IBIS-AMI**

Sim Result

- **Reference Cable+BP**
- **PKG Model**
- **PCB Model**

- **S-Para**

Compliance Test Simulation Kit

- **Assign**

At the actual design

- **Ball Assign'**
- **PCB Artwork'**

Customer Design

- **PKG Model'**
- **PCB Model'**

- **S-Para**

Compare

Differential Analysis

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Measurement Correlation (1/2)

Measurement environment

<table>
<thead>
<tr>
<th>Item</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP</td>
<td>USB3.0 Test Chip</td>
</tr>
<tr>
<td>PKG</td>
<td>Wire Bond BGA 4layer 256ball 27mm-square</td>
</tr>
<tr>
<td>PCB</td>
<td>6layer</td>
</tr>
<tr>
<td>PVT</td>
<td>Typical</td>
</tr>
</tbody>
</table>
Measurement Correlation (2/2)

Measurement vs Simulation

Models of Test Chip
We can examine cost reduction of the product by using Simulation Kit in a short TAT.
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USB3.0 Compliance Simulation using IBIS-AMI Model

- IBIS-AMI is a key technology of 5Gbps SerDes I/F analysis.
  - High accuracy
  - Short TAT

- It is important that IBIS-AMI model maker solve various problems between IBIS-AMI and EDA tool beforehand.

- Simulation Kit constructed on EDA tool is able to contribute to short TAT analysis and cost reduction of the product.

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Expectation of IBIS-AMI

- We expect more information about IBIS-AMI.
  - Documents (IBIS-AMI Cookbook, Trouble shooting)
  - Samples (IBIS-AMI, Simulation result)
  - Visualization (EQ Characteristic)