DDRn Interface Signoff Analysis with Distributed Chip IO Interconnect Model

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Introduction About the Chip IO Interconnection

Chip IO Interconnect Model Extraction and Analysis

Case Study – DDR SSO and Chip IO Power Decap

Summary
Simplified View of a Smartphone Board

PoP (LPDDR2) + eMMC
PoP (LPDDR3) + eMMC

eMCP (LPDDR2+ eMMC)
eMCP (LPDDR3+ eMMC)

4Gb eMMC +8Gb LPDDR2 Memory
eMCP (LPDDR2+eMMC) 11.5x13x1.0mm3 162b FBGA 0.5mm pitch
12x12 PoP + eMMC only 11.5x13x1.0mm3 153b FBGA 0.5mm pitch

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Chip IO interconnection Structure
DDRn System Interconnection Topology

Chip Model = Distributed IO
Power/Ground/Signal
Interconnect Model (from M1 to Bump)

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Uncertainties Vs Timing Margin

Transmitter

DQ

Setup

Hold

DQS

Receiver

DQ

Setup Margin

Hold Margin

DQS

DQ Eye Between AC Thresholds

Set Up Uncertainty

Set Up Margin

Hold Margin

Hold Uncertainty

Total Eye Width = 1 Unit Interval

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## DDRn Setup/Hold Timing Budgets

(Uncertainties : Skew & Jitter)

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Contributions</th>
<th>Interconnection Contributions</th>
<th>Receiver Contributions</th>
</tr>
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<tbody>
<tr>
<td>DLL (Data Delay Line) Granularity and bit offset (BDL and LCDL) (Static)</td>
<td>Signal Length Mismatches (On-chip interconnection M1 to Bump, RDL Routing, Package Substrate and PCB layout Skew) (Static)</td>
<td>Input Rise/Fall Slew Factor (Static)</td>
<td></td>
</tr>
<tr>
<td>Register Mismatch within the PHY (Static)</td>
<td>Crosstalk (Pushout/Pullin from nearby aggressor signals and serpentine routing) (Dynamic)</td>
<td>DDRn Data Set Up and Hold specifications (tDS, tDH) (Static)</td>
<td></td>
</tr>
<tr>
<td>DLL Jitter including Clock Source Jitter (Dynamic)</td>
<td>Reflections, Inter-Symbol Interference (ISI) (Impedance discontinuities, topology, loading) (Dynamic)</td>
<td>Setup and Hold Slew rate Derating (Static)</td>
<td></td>
</tr>
<tr>
<td>DLL Phase Error (Dynamic)</td>
<td>High frequency losses (Dielectric and Conductor losses) (Dynamic)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PHY Skew between DQS/DQS# and DQ signals (Static)</td>
<td>Dielectric mismatches between layers (Dynamic)</td>
<td></td>
<td></td>
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<tr>
<td>Process Variation Effects (Static)</td>
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<td></td>
<td></td>
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<tr>
<td>IO Output Rise Fall Delay Mismatch (Static)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSO/SSN Pushout (Effects of non-ideal power distribution network-PDN) (Dynamic)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VT Drift (BDL and LCDL Setting) (Dynamic)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**Inputs**
- LEF/DEF or GDS
- Technology file (.ict)
- Layer map file

**Outputs**
- IO interconnect model
  - SPICE netlist
- EPA results
  - Power pin RL
  - Power net capacitance
  - Power net impedance
  - Signal net RLC
  - Signal net return and insertion loss
Chip Model Parts

Transistors Model
- IO Transistor to Behavior Model (IBIS)
- IBIS v5 and IBIS Plus Model

ASIC GDS
- Chip IO Interconnect Model Extraction
- SPICE Netlist

PKG MCM
- Package Model Extraction
- SPICE Netlist

The Chip Description

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Chip IO Model Add in the IBIS Model Simulation

Chip IO Model Add in the IBIS Model Simulation

IBIS + Chip IO model + PKG

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Chip IO interconnect model includes signals and IO pwr/gnd
Chip IO interconnect model is extracted by chip level extractor which include RLCK elements.
PCB and package are extracted by EM solver and converted into broadband SPICE model.
Test vehicle of system level SI/PI analysis (DQ/DQS)

Chip IO interconnection model extraction

Package merged with PCB
Power aware signal integrity analysis
System level SI/PI analysis (DQ/DQS) with memory write in TD—ODT40
Power aware signal integrity analysis
System level SI/PI analysis (DQ/DQS) with memory write in TD—ODT60

Eye Diagram

Bank0

Voltage (V)

Time (ns)

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Test vehicle of system level SI/PI analysis coupling among ADD/CMD/CLK and DQ/DQS

Package merged with PCB
Build ADD/CMD/CLK and bank0 groups

Chip IO model extraction
Test vehicle of system level SI/PI analysis coupling among ADD/CMD/CLK and DQ/DQS

- Running DQ/DQS patterns first then turn on ADD/CLK.
- To measure ADD/CLK lines noise while DQ/DQS are toggling.
- To monitor ADD/CLK waveform and see if they are affected by DQ/DQS.
- All DQ/DQS are in ODT-off.

<table>
<thead>
<tr>
<th>Bus Group/Signal</th>
<th>Stimulus Pattern</th>
<th>Stimulus Offset (ns)</th>
<th>Transmit IO Model</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR1</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Not Connected</td>
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<tr>
<td>ADDR2</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>ADDR3</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<td>ADDR4</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<td>ADDR5</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<td>ADDR6</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<td>ADDR7</td>
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<td>ADDR8</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>ADDR9</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>ADDR10</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>ADDR11</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>se_driv15_odt/off</td>
<td>Signal</td>
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<td>ADDR13</td>
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<td>Signal</td>
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<td>ADDR14</td>
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<td>Signal</td>
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<td>ADDR15</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>BA0</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>BA1</td>
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<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>BA2</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
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<td>CASN</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>CKE</td>
<td>0000000000000000110011000111000011100011001100..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>CS_N</td>
<td>0000000000000000110011000111000011100011001100..</td>
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<td>se_driv15_odt/off</td>
<td>Signal</td>
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<td>dm0</td>
<td>010100110011000100110..</td>
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<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>dm1</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
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<tr>
<td>dq0</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
</tr>
<tr>
<td>dq1</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
</tr>
<tr>
<td>dq2</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
</tr>
<tr>
<td>dq3</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
</tr>
<tr>
<td>dq4</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
</tr>
<tr>
<td>dq5</td>
<td>010100110011000100110..</td>
<td>0</td>
<td>se_driv15_odt/off</td>
<td>Signal</td>
</tr>
</tbody>
</table>

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Coupling among bank0 and ADD/CMD (measured at U1)

Voltage (V)

VDDQ15 noise

DQ0

ADDR0

Diff: 0.193897 (V)
Coupling among bank0 and ADD/CMD (measured at U3)
Chip Decap What-if Analysis and Optimization

- Ports for IO cells which can be impedance observations
- Ports for PSCAP/MOS cap cells which can be decaps and optimized
Power integrity analysis

4 types of MOS cap value

ID=23

ID=24

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Power integrity analysis
--1st stage MOS caps optimization on chip

ID=25

ID=26

4 types of MOS cap value
Power integrity analysis

-- 1st stage MOS caps optimization on chip

MOS caps with 200pF for each cell will have best impedance profile
• This is the definition of big cell with x7 small and x1 large cells
• Total value for this big cell is ranging from 20,50,80,200PF.
• A strongly recommendation that places MOS caps as much as possible
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Summary
Summary

• Chip IO interconnect model should include IO Power/Ground/Signal Interconnect Model

• For high speed and low power DDR systems (LPDDR3/DDR3L/DDR4), Chip IO interconnect model is crucial for IO-SSO analysis.

• Chip IO interconnect model is one part for Chip but not in IBIS model.

• With Chip IO Interconnection model, Chip vendor can do more accurate DDRn signoff analysis to predict System electrical performance before ASIC tapeout.

• On-die RC or better distributed chip IO interconnect model can be more realistic for signal/power analysis

• New System Signoff methodology enable to avoid overdesign or under-design for on-die Decap Cell
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