IBIS Modeling for IO-SSO Analysis

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Agenda

What is IO-SSO?

Missing Components in Traditional IO-SSO Analysis

Accurate On-die and Package Effects in IBIS Models

Creating IBIS Models with On-die Interconnect

Case Study – IO-SSO Analysis with IBIS Models

Summary
What is IO-SSO?

- A DDR memory interfaces is a parallel bus
  - Many signals represent a data byte/word/32-bit word/64-bit word
  - Simultaneous switching signals / outputs are referred to as SSO
  - The noise between power and ground created is referred to as simultaneous switching noise (SSN)
  - IC Designers refer to this phenomenon as IO-SSO
- SI/PI can be verified by IO-SSO
IO-SSO Impacts Timing and Noise Margin

- Data transfers are faster and more sensitive to instability of the PDN
  - DDR runs at 2.5 V
  - DDR2 runs at 1.8 V
  - DDR3 runs at 1.5V
  - DDR4 to run at 1.2 V – 1.05V

SSN effects impact timing and noise budget:

- Decreasing Timing Budget
  - ±600ps ➔ ±300ps ➔ ±150ps

Ground bounce Peaks and Valleys must be minimized with low signal voltages.
Higher Data Rate ➔ High Level Interactions

Electrical and Physical worlds collide requiring multi-fabric simulation

Increased interaction between signals

Increased interaction between system hardware components
Traditional IO-SSO Simulation Scenarios

- Pessimistic result when analyzed without on-die model.
- Optimistic result when analyzed with estimated on-die model.

**Red:** Pessimistic without chip IO interconnect model

**Blue:** Optimistic with chip simple capacitor model
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Missing Components in Traditional IO-SSO Analysis

- Post-sim transistor SPICE netlist only includes limited parasitic information.
- Distributed behavior of IO’s P/G impedance can’t be represented.
- Pin Mapping table may not be defined accurately.
- On-die decap model is not captured in IBIS model.
- All above problems make IO-SSO simulation lose accuracy.
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- Chip PDN model is crucial for IO-SSO analysis.
- Without Chip PDN model, artificially large power/ground noise impact the signal waveform significantly.
- Chip PDN is responsible to filter high frequency noise.
- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis.
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Adding On-die Effects to the IBIS Model

Buffer + Chip IO model + PKG
Connecting Buffer, On-Die and Package Models

**IBIS 5.1**

- Effectively incorporates the on-die and package models into the buffer.
- The package and on-die models may be of arbitrary topology to include coupling, non-ideal power deliver and other effects.
- Applying IBIS 5.1 [External Circuit] sub-components is similar to sub-circuit call and connections in HSPICE.
- Future ISS based solution may be coming from committee.
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Creating IBIS Models with On-die Interconnect (1/4)

• Generate chip IO model
  – LEF/DEF or GDSII data can represent physical geometry.
  – Includes Power/Ground/Signal routing with On-Die caps.
  – Define Chip stackup, circuit mapping
  – Chip IO model extraction is based on chip layout which includes metal_x to the top layers (x can be 1~N). Model builder needs to be aware what SPICE nest-list is from pre-sim or post-sim flow.
  – Generate SPICE netlist
• [External Circuit] will be represented as IO buffer, chip IO, package.....
• Connect each [External Circuit] through [Circuit Call]
Creating IBIS Models with On-die Interconnect (3/4)

• Ports under [External Circuit]

The [External Circuit] keyword allows the user to define any number of ports and port functions on a circuit.

Port name for IO Buffer

Ports A_puref A_pdref A_signal A_drive
A_enable A_receive A_pcref A_gcref

Ports vcca1
Ports vcca2

...........
- Define [Pin] and [Node Declarations]
  - When a [Circuit Call] keyword defines any connections that involve one or more die pads (and consequently pins), the corresponding pins on the [Pin] list must use the reserved word “CIRCUITCALL” in the third column instead of a model name.
  - [Node Declaration] provides a list of internal die nodes and/or die pads for a [Component] to make unambiguous interconnection descriptions possible

```
[Node Declarations]     | Must appear before any [Circuit Call] keyword
| Die nodes:             | List of die nodes
pu1 pd1 io1p io1 in1 en1 outin1  | List of die nodes
pu2 pd2 io2p io2 in2 en2 outin2  | List of die nodes
pu3 pd3 io3p io3 in3 en3 outin3  | List of die nodes
[End Node Declarations]
```
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- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary
Case Study – IO-SSO Analysis with IBIS Models

- I/O transistor circuit is converted into power-aware IBIS model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package S-parameters are extracted and converted to broadband SPICE models.
- Only 1 group DDR data is considered for this test
Case Study – IO-SSO Analysis with IBIS Models

- SSN from SSO will be over or underestimated without accurate chip IO model.
- Timing push in/out will become worse if more IOs are switching at the same time.

RED: without chip PDN
Green: with on-die RC
Blue: with distributed broadband model

28.5 ps
29.1 ps
740 mV
117 mV
46 mV

\text{V_{REF(d)} = 0.9 (V)}
IR drop becomes worse after including chip IO model.

• Noise level at each IO pad is different, which reveals the distributed behavior of the IO power deliver network.
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• For tighter timing and noise budgets in LPDDR3 or DDR4, system level IO-SSO analysis is helpful for design margin assessment

• IBIS 5.1 models may include power-aware IO buffer, chip P/G/S from IOs to bump pads, and arbitrary package models
  - existing IBIS syntax is applied (using [External Circuit])
  - additional techniques using ISS within the IBIS model are being discussed in committee

• The approach described allows chip vendors to deliver more complete IBIS models to their customers to enable faster and more accurate product design verification