Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion
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- Problem Statement
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Problem Statement
- Certify Controller IBIS models before system simulations

- DDR compliance needs to be done on a system interconnect starting from Controller to Memory IO
- If DDR IBIS models do not adhere to DDR JEDEC standards, designer may wrongly associate performance issues with interconnect elements like board, connector, DIMMs, package.
- It is important that we decouple the testing into
  - Testing of IBIS models to make sure they comply with JEDEC standards
  - Testing of interconnect elements with above certified IBIS models
Problem Statement
- Do exhaustive checks on IO netlist performance

- Simulating IO-netlists for all corners to verify compliance against JEDEC specs is time-consuming.

- Since IBIS modeling is an automated process, the generated IBIS model can quickly provide results that can be verified against JEDEC requirements (for all corners and impedance settings) like
  - Impedance variation
  - Slew rates
  - Pulse-width variation
  - ZQ calibration based on process corners
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Overview of DDR compliance checks - JEDEC DDR4 spec (output impedance)

Spec indicates impedance measurement to be done at different Vout levels and that they should be within +/- 10%
Overview of DDR compliance checks
- Single-ended slew rate

<table>
<thead>
<tr>
<th>Description</th>
<th>Measured</th>
<th>Defined by</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single ended output slew rate for rising edge</td>
<td>Vol(AC)</td>
<td>[rac{[V_{OH}(AC)-V_{OL}(AC)]}{\Delta T_{Rse}}]</td>
</tr>
<tr>
<td>Single ended output slew rate for falling edge</td>
<td>V_{OH}(AC)</td>
<td>[rac{[V_{OH}(AC)-V_{OL}(AC)]}{\Delta T_{Fse}}]</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

**Figure 182 — Single-ended Output Slew Rate Definition**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>DDR4-1600</th>
<th>DDR4-1866</th>
<th>DDR4-2133</th>
<th>DDR4-2400</th>
<th>DDR4-2666</th>
<th>DDR4-3200</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single ended output slew</td>
<td>SRQse</td>
<td>4</td>
<td>9</td>
<td>4</td>
<td>9</td>
<td>4</td>
<td>9</td>
<td>TBD</td>
</tr>
</tbody>
</table>

**Spec indicates that DQ slew rate should be within Min and Max values**
Overview of DDR compliance checks - Differential slew rate

<table>
<thead>
<tr>
<th>Description</th>
<th>Measured</th>
<th>Defined by</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential output slew rate for rising edge</td>
<td>( V_{OH_{diff}}(AC) )</td>
<td>( \frac{[V_{OH_{diff}}(AC)-V_{OL_{diff}}(AC)]}{\Delta TR_{diff}} )</td>
</tr>
<tr>
<td>Differential output slew rate for falling edge</td>
<td>( V_{OL_{diff}}(AC) )</td>
<td>( \frac{[V_{OH_{diff}}(AC)-V_{OL_{diff}}(AC)]}{\Delta TF_{diff}} )</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

**Figure 183 — Differential Output Slew Rate Definition**

**Table 79 — Differential output slew rate**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>DDR4-1600</th>
<th>DDR4-1866</th>
<th>DDR4-2133</th>
<th>DDR4-2400</th>
<th>DDR4-2666</th>
<th>DDR4-3200</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>Differential output slew rate</td>
<td>SRQdiff</td>
<td>8</td>
<td>18</td>
<td>8</td>
<td>18</td>
<td>8</td>
<td>18</td>
<td>TBD</td>
</tr>
</tbody>
</table>

Spec indicates that DQS slew rate should be within Min and Max values
Overview of DDR compliance checks - Pulse-Width@data-rate

<table>
<thead>
<tr>
<th>Speed</th>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Clock Timing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minimum Clock Cycle Time (DLL off mode)</td>
<td>tCK (DLL_OFF)</td>
<td>8</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Average Clock Period</td>
<td>tCK(avg)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>Average high pulse width</td>
<td>tCH(avg)</td>
<td>0.48</td>
<td>0.52</td>
<td>0.48</td>
<td>0.52</td>
<td>0.48</td>
<td>0.52</td>
<td>tCK(avg)</td>
</tr>
<tr>
<td></td>
<td>Average low pulse width</td>
<td>tCL(avg)</td>
<td>0.48</td>
<td>0.52</td>
<td>0.48</td>
<td>0.52</td>
<td>0.48</td>
<td>0.52</td>
<td>tCK(avg)</td>
</tr>
<tr>
<td></td>
<td>Absolute Clock Period</td>
<td>tCK(abs)</td>
<td></td>
<td></td>
<td>tCK(avg)min + tJ IT(per)min to t</td>
<td>tCK(avg)m ax + tJ IT(per)m ax tot</td>
<td>tCK(avg)min + tJ IT(per)min to t</td>
<td>tCK(avg)m ax + tJ IT(per)m ax tot</td>
<td>tCK(avg)</td>
</tr>
<tr>
<td></td>
<td>Absolute clock HIGH pulse width</td>
<td>tCH(abs)</td>
<td>0.45</td>
<td>-</td>
<td>0.45</td>
<td>-</td>
<td>0.45</td>
<td>-</td>
<td>tCK(avg)</td>
</tr>
<tr>
<td></td>
<td>Absolute clock LOW pulse width</td>
<td>tCL(abs)</td>
<td>0.45</td>
<td>-</td>
<td>0.45</td>
<td>-</td>
<td>0.45</td>
<td>-</td>
<td>tCK(avg)</td>
</tr>
</tbody>
</table>

Spec indicates that the duty cycle should be greater than .45UI
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Methodology to check DDR compliance
- IBIS impedance measurement (pulldown)

- IV curves of IBIS can be plotted to ensure that they fall within +/- 10% tolerance
Methodology to check DDR compliance - pullup

- IV curves of IBIS can be plotted to ensure that they fall within +/- 10% tolerance
Methodology to check DDR compliance - Impedance check

- IV plots from IBIS being compared against 10% limits
Methodology to check DDR compliance
- Single ended slew rate measurement test-bench

- Figure shows simple drive of IO buffer with 50ohms pull-up to capture the rise time.
Falling slew rate $\frac{dv}{dt}$

Here $\frac{dv}{dt} = 360\text{mV}/65\text{pS} = 5.6 \text{ V/ns}$ which is within spec of 4 to 9 V/ns
Rising slew rate

Here \( \frac{dv}{dt} = \frac{360 \text{mV}}{54 \text{pS}} = 6.6 \text{ V/ns} \) which is within spec of 4 to 9 V/ns
Methodology to check DDR compliance - Differential test-bench (DDR4)

- Figure shows simple drive of differential IO buffer with 100 ohms termination to capture the rise and fall time.
Falling Slew Rate

Here \( \frac{dv}{dt} = \frac{722 \text{mV}}{73 \text{pS}} = 9.9 \text{ V/ns} \) which is within spec of 8 to 18 V/ns.
Rising Slew Rate

Here \( \frac{dv}{dt} = 722\text{mV}/80\text{pS} = 9.0 \text{ V/ns} \) which is within spec of 8 to 18 V/ns
Methodology to check DDR compliance  
- Timing Checks

- Average High Pulse
- Average Low Pulse
- Average Clock Period
Data Pulse variation @ 3.2G (slow corner)

Here min duty cycle is \( \frac{312\text{pS}}{625\text{pS}} = 0.499\text{UI} > 0.45\text{UI} \)
Here min duty cycle is $309\text{pS}/625\text{pS} = 0.494\text{UI} > 0.45\text{UI}$
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Conclusion

- It is important to verify DDR controller IBIS separately before doing system simulations.
- IBIS verification against JEDEC requirements can help in:
  - Quickly verifying PHY netlist for compliance.
  - Ensuring that IBIS models have been correctly made with proper netlist settings, especially when ZQ calibration needs to be properly done to obtain proper impedance values at corners.