True Differential IBIS model for SerDes Analog Buffer

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Agenda

- Overview of Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion
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Overview of Differential IBIS
- Current approaches

- Traditionally, differential buffer have been modeled as
  - Pseudo Differential buffer using two Single-ended IBIS models
    - Accuracy can suffer if there is substantial differential current which is the case with Serial Link analog buffers that has series elements between PADP and PADN
  - External Model approach: Call to buffer netlist
    - Netlist (IP) needs to be revealed
  - External Model approach: Call to S-parameter model
    - Rx buffer needs to be characterized as S-parameters
Overview of Differential IBIS
- Alternate approach

- While S-parameter approach is best suited for analog buffers in serial links, we provide an alternate way to model it through standard IBIS tabular format with use of series elements to model differential current.

- This extends the approach suggested in IBIS cookbook that suggests modeling of differential current using series Resistance.
  - Here we propose use of reactive elements (R/L/C) to model differential current.
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Description of test-case
- IBIS modeling of Serial Link RX IO

- 10Gbps Serial link
- 28nm technology node
- Typical process node
- Rx analog buffer had additional blocks for equalization that were modeled as AMI code
  - Frontend attenuation
  - VGA
  - CTLE
  - DFE
  - CDR
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Flow used to create differential IBIS model
- True differential

Setup for common mode and differential mode impedance extraction
Flow used to create differential IBIS model
- True differential

\[ I_{\text{Diff}} = I_{AC}(V_{DC}) \]
\[ I_{\text{Comm}} = I_{AC}(V_{AC}) - I_{AC}(V_{DC}) \]

- \( I_{\text{Diff}} \) flows through series element between inverting and non-inverting pins
- \( I_{\text{Comm}} \) flows only through common mode impedance
Flow used to create differential IBIS model
- True differential buffer with series element $Z_{\text{series}}$

Output Buffer

Input Buffer
Flow used to create differential IBIS model
- Differential and common mode impedance calculations

- Series Reactance: \( X_{series} = \frac{V_{AC}}{\text{Im}(I \_ \text{Diff})} \)

- Series Resistance: \( R_{series} = \frac{V_{AC}}{\text{Re}(I \_ \text{Diff})} \)

- Common mode Resistance: \( R_a = \frac{V_{AC}}{\text{Re}(I \_ \text{Comm})} \)

- Common mode Reactance: \( X_a = \frac{V_{AC}}{\text{Im}(I \_ \text{Comm})} \)
Flow used to create differential IBIS model
- Differential and common mode impedance calculations

• Depending on sign, reactance could be inductive or capacitive

• Impedance to be calculated at most likely operating frequency of buffer

• For 10G serial link Rx buffer testcase

<table>
<thead>
<tr>
<th></th>
<th>R=220ohms</th>
<th>L=9.8nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series Model</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common mode Model</td>
<td>R=80ohms</td>
<td>C=0.223pF</td>
</tr>
</tbody>
</table>
### Common mode and differential currents

- **Re($I_{\text{Diff}}$)**
- **Im($I_{\text{Diff}}$)**
- **Re($I_{\text{Comm}}$)**
- **Re($I_{\text{Diff}}$)**
Flow used to create differential IBIS model
- IBIS model

Parallel RL network present as Zseries, modeled using “Model_type Series”
Flow used to create differential IBIS model
- IBIS model

```
[Model]    Rx_in
Model_type  Input
Vinl=1.5
Vinlh=2.5
| variable      typ  min  max
|-------------------------
| C_comp            0.223pF  NA  NA
[Temperature Range]  70   NA   NA
[Voltage range]      3.3  NA   NA

```

- Parallel RC network present as Zcomm, modeled using clamp I-V table and C_comp
Agenda

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Comparison: Pseudo-differential vs. True-Differential IBIS simulations

- Serial Link Simulation Test-bench
  - 10Gbps
  - No Equalization
  - PRBS23
  - Tested on different channels
Channel 1

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Insertion Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.15GHz</td>
<td>-5.861dB</td>
</tr>
</tbody>
</table>

![Graph showing the insertion loss across different frequencies. The graph has a grid with the x-axis labeled 'Frequency (GHz)' ranging from 2 to 12 GHz, and the y-axis labeled 'S Amplitude (dB)' ranging from 0 to -14 dB. The line graph starts at 5.15 GHz with an insertion loss of -5.861 dB and shows a decrease in amplitude as frequency increases.]
## Channel 2

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Insertion Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1GHz</td>
<td>-4.14dB</td>
</tr>
</tbody>
</table>

![Graph showing frequency vs. insertion loss](image)
Comparison: Pseudo-differential IBIS vs. True-Differential IBIS vs. Circuit simulations

- Channel 1
Comparison: Pseudo-differential IBIS vs. True-Differential IBIS vs. Circuit simulations

- Channel 2
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Conclusion

- Extended “Series Model Approach” in Cookbook for IBIS Version 4.0 to model differential and common-mode impedances for SERDES analog buffer.
- True differential model provides much better accuracy than pseudo differential IBIS for channel simulations in terms of
  - Jitter and eye opening
  - Reflection losses