Introduction of P2401 LSI-Package-Board Standard Format

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LSI Package Board needs…

- Mutual Communication
- Design Consistency
- Shorten Development Time

Enabled by

New Standard format
About LPB-WG

Semiconductor board
Electronic Design Automation Technical Committee
LPB (LSI Package board) interoperable design process working group


• Members

• LPB-WG + ex-LPB-WG
  Toshiba, Fujitsu semiconductor, Renesas Electronics
  Canon, Sony, Panasonic, Denso, Nokia
  Fujitsu VLSI, Sony LSI, NEC System Technologies
  Toppan NEC Circuit solutions
  Zuken, Cadence Japan, Mentor Graphic Japan, StayShift(nimbic)
  Fujitsu Advanced Technologies, Gem Design Technologies.
  ANSYS, ANSYS Apache, ATE service(Sigrity), etc.
• Product development flow & EMC issues

**Issues**

- **Product planning**
- **Circuit Design**
- **Layout**
- **SI/PI/EMC Check**
- **Manufacturing**
- **Compliance / Field Test**

**Current**

Time consuming, re-design at all => development cost, missing business window
How to improve…

- Improve - put check point from early stage,
  - IBIS Sim
  - IBIS Sim
  - IBIS Sim
  - IBIS Sim

Reduce iterations
=> Time to market
Challenge of EMC simulation in design

- To estimate simulation time which is allowed in each design steps

Allowable Simulation time:

- Product planning: 0.5 h
- Circuit Design: 1 h
- Layout: 3 h
- SI/PI/EMC Check: 3 days
- Manufacturing: 1~3 week
- Compliance/Field Test:

Allowable simulation times are different in the development stage.
What is the simulation time?

- definition

Simulation time = 

Parameter collection + setup + calculation

Meeting, e-mail, negotiations hand mesh, method, hard

Typical TAT

2 weeks 1 day 30 hours
However...

- Actually …

Allowable Simulation time

IBIS simulation cannot be done at early stage.
Challenge to reduce the time. But...

<table>
<thead>
<tr>
<th>Parameter collection</th>
<th>setup</th>
<th>calculation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meeting, e-mail, negotiations</td>
<td>hand</td>
<td>mesh, method, hard</td>
</tr>
</tbody>
</table>

2 weeks \[\Rightarrow\] 1 day | EDA / computer / Academic challenge

3D view: Port definition
Test pulse excited at port 11

3D view: Port definition

supplied by OR tech

- Simulation time < 97 sec / port
- Memory usage 680 MB
- 13 Million cells; grid: 15 μm < Δ < 200 μm
- Used CPU: Intel Xeon E5-2687W
Still...

- Not enough ...

Allowable Simulation time

Still ...IBIS simulation cannot be done at early stage.
What LPB is trying to achieve?

Parameter collection | setup | calculation

2 weeks | 1 day | EDA / computer / Academic challenge

Common formats

List of information, exchange format, common terms & definitions

Community / e-commerce

Extremely shorten total simulation time
Finally!

Reach to the target!

- Product planning
- Circuit Design
- Layout
- SI/PI/EMC Check
- Manufacturing
- Compliance / Field Test

Optimization time

IBIS Sim verification

1~3 weeks

IBIS simulation can be done from early stage.
Design and Simulation

- LPB Standard format is also effective to shorten design process.
Design and Simulation

- LPB Standard format is also intended to shorten design process.

Product planning  Circuit  Layout  SI/PI/EMC Check  Manufacturing  Compliance/Field Test

IBIS Sim  IBIS Sim  IBIS Sim  IBIS Sim

Sim final check

Quality + Time to market
JEITA LPB-WG produce LPB Standard format.

Design environment to be constructed by 6 formats,
1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary
LPB standard format reveal what the information necessary. The required information must be shared and are provided in the supply chain.
LPB Community

http://www.lpb-forum.com/

- User/EDA/Suppliers community

**EDA vendors**
- CAD CAE
- Develop LPB interface

**Users/Designers**
- Semiconductor Electronics products
- Implement LPB design flow

** Suppliers**
- Package, PWB, Passive, Connectors, etc.
- Deliver design rule parametric data
- With LPB format.

LPB Standard format is promoted as for ‘Forum Standard’.

- Seminar

- Standardization committee
  - JEITA EDA-TC/LPB-WG

Exhibit

Release/Update

Feedback

Sponsor
Approved project: P2401 LPB-WG
IEC dual logo : follows P2401
EDA vendors adoption

• More than 10 vendors already start to develop LPB interface.

• In addition, Mentor/ Cadence/ Fujitsu advanced technologies are also member of standardization committee of LPB.
LPB Standard Format
& Usage example
Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary
## LPB Standard Format Abstract

<table>
<thead>
<tr>
<th>Format</th>
<th>Abstract</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| **Project Management (M-Format)** | Manage the LPB files of the LSI, package and board.  
- Manage the history, revision and update of the files  
- JEITA original format using XML | Easy to Manage Design history  
Easy to understand Design Status  
Understanding The Latest Condition for Verification |
| **Netlist (N-Format)** | Connection of the parts  
- Netlist between LSI, Package and Board.  
- Verilog HDL format | Easy to Check Connection Between LSI-PKG-Board  
Enable to Simulate on Board Level |
| **Component (C-Format)** | Information of the parts that includes  
- Pin assignment  
- Design constraint  
- Design Status  
- JEITA original format using XML | Easy to Verify for Optimization of LPB  
Clarification of Constraint Condition |
| **Design Rule (R-Format)** | Rules of the components that includes  
- Design rule  
- Assembly rule  
- Characteristics of the material  
- JEITA original format using XML | Clarification of Design Rule in Advance  
Clarification of Verification Condition  
Easy to Set up for Verification |
| **Geometry (G-Format)** | Geometry of the Package and Board  
- XFL format | Efficient Use of Design Property  
Use as Reference Design  
Easy to convert Data |
Project Manage (M-Format)

Abstract

- Manage the LPB files of the LSI, package and board.
- Manage the history, revision and update of the files
- JEITA original format using XML

Example

```
<include MFORMAT="MFMT_FKB48.xml" />
<include MFORMAT="MFMT_SOC_PKG.xml" />

<class comment="DDR MEMORY" >
  <CFORMAT file_name="CFMT_DDR.xml" />
  <RFORMAT file_name="RFMT_DDR.xml" />
  <NFORMAT file_name="NFMT_DDR.v" />
  <OtherFile file_name="DDRPowerModel.sp" />
</class>
```
### LPB Standard Format Abstract

#### Netlist (N-Format)

**Abstract**
- Connection of the parts
- Netlist between LSI, Package and Board.
- Verilog HDL format

**Example**

```verilog
module JEITA_SAMPLE ( );
    wire [23:0] FKBDO ;
    wire [23:0] FKBDI ;
    wire VDD33 ; /* PG_NET */
    wire DGND ; /* PG_NET */

    FKB48 FKB48 ( .AIN(FKBDO),   .AOUT(FKBDI) ) ;
    SOC_PKG SOC ( .FKBDO(FKBDO), .FKBDI(FKBDI) ) ;

endmodule
```
## Component (C-Format)

### Abstract

Information of the parts that includes:
- Pin assignment
- Design constraint
- Design Status
- JEITA original format using XML

### Example

```xml
<module name="SOC_PKG" type="PKG" shape_id="PKG_BODY" >
  <socket name="SOC_PKG" >
    <port id="A5"  x="-8500"  y="12500"  angle="0"  name="FKBDO[5]" /> 
    <port id="A6"  x="-7500"  y="12500"  angle="0"  name="FKBDO[2]" /> 
    <constraint> 
      <impedance group_name="FKB_DIN"  type="single"  min="40"  typ="50"  max="60"/> 
      <delay group_name="FKB_DIN"  min="100"  typ="150"  max="200" />
    </constraint>
  </socket> 
</module>
```
LPB Standard Format Abstract

Design Rule (R-Format)

Abstract
Rules of the components
- Design rule
- Assembly rule
- Characteristics of the material
- JEITA original format using XML

Example

```xml
<material_def>
  <conductor material="COPPER" volume_resistivity="1.68e-8" />
  <dielectric material="FR-4" permittivity="4.5" tan_delta="0.035" />
</material_def>

<layer_def>
  <layer name="TOP_COND" type="conductor" thickness="0.030"
        conductor_material="COPPER" />
  <layer name="DIELECTRIC12" type="dielectric" thickness="0.100"
        dielectric_material="FR-4" />
</layer_def>

<spacing_def>
  <layer name="TOP_COND">
    <line_to_line space="0.050" />
  </layer>
</spacing_def>
```
## Geometry (G-Format)

<table>
<thead>
<tr>
<th>Abstract</th>
<th>Geometry of the Package and Board</th>
<th><img src="image" alt="Diagram" /></th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>shape 1 4 53.2 26.8 90 N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>via 1 4 V020C060C085 54.55 20 0 N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>via 2 3 B010C050C075C23 41 24.25 0 N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>shape 1 11 35.5 29 0 N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>via 1 2 B010C030C12 35.5 29 0 N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>path 2 0.1 {</td>
<td></td>
</tr>
<tr>
<td></td>
<td>41 24.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td>41.000000 24.750000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>}</td>
<td></td>
</tr>
</tbody>
</table>
LPB Files Delivery

- **C-Format**
  - Die models
  - IBIS/SPICE
  - CPM/LPM
  - Die Size
  - Pad location
  - Spice Model correspondence

- **C-Format**
  - Package size
  - Terminal location
  - Spice/IBIS/S-param model correspondence

- **C-Format**
  - Outline
  - Terminal location
  - Simulation model correspondence

- **N-Format**
  - Connectivity
  - Die mount rotation
  - Flip

- **M-Format**
  - Revision number of Each N/C/R/G files

- **G-Format**
  - PKG routing/Plane/Bond wire

- **R-Format**
  - Line/Space
  - Via pitch/size/hole
  - Layer Stuck up
  - Material parameter

- **R-Format**
  - Wire Bonding rules

- **LPB Files Delivery**
  - C-Format
  - R-Format
  - M-Format
  - N-Format

- **Analysis**
  - Auto set-up simulation project

- **Simulation model**
  - S-param
  - SPICE etc

- **Design**
  - Package size
  - Terminal location
  - Spice/IBIS/S-param model correspondence

- **Die mount rotation**
  - Flip

- **连接性**
  - N-Format

- **M-Format**
  - Revision number of Each N/C/R/G files

- **G-Format**
  - PKG routing/Plane/Bond wire
LPB sample files for test bench

Golden Sample are provided as a test bench for implementation.
Reference flow using LPB standard format

To understand the function of the LPB standard format.
### Growth of LPB files in design steps

<table>
<thead>
<tr>
<th>C-Format</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>header</td>
</tr>
<tr>
<td>Global</td>
<td>unit: Defines the unit shape, shape: Defines the shape, pad stack: Defines the pad stack</td>
</tr>
<tr>
<td>Module</td>
<td>socket: Defines the input/output ports of the module, port: Defines the port shape, name and location, port group: Defines the group of the ports, power domain group: Defines the power domain of the signals, swappable port/group: Defines the swappable ports/port groups, frequency: Specifies the operating (clock) frequency for the port, constraint: Defines the constraints for the upper hierarchy, specification: Defines the specification of the module, reference: Defines the connection procedure between ports in socket section and ports in referenced file.</td>
</tr>
<tr>
<td>Component</td>
<td>placement: Defines the placement of the module</td>
</tr>
</tbody>
</table>

**Placement Information of the parts**

[Example]

```xml
<placement ref_module="SOC" inst="SOC" x="400" y="-6500" />
<placement ref_module="DDR" inst="DDR0" x="37000" y="-3200" />
```

LPB files will grow every time you go through the process of the design.
<Example> The growth of C-format

LPB files grow and share the information each other.
**Example** The growth of C-format

```xml
<!-- Swappable Group -->
<swappable_group>
  <ref_portgroup name="FKB_DIN_BYTE0"/>
  <ref_portgroup name="FKB_DIN_BYTE1"/>
  <ref_portgroup name="FKB_DIN_BYTE2"/>
</swappable_group>

<!-- Swappable Port -->
<swappable_port>
  <ref_port name="FKBDO[0]"/>
  <ref_port name="FKBDO[1]"/>
  <ref_port name="FKBDO[2]"/>
  <ref_port name="FKBDO[3]"/>
  <ref_port name="FKBDO[4]"/>
  <ref_port name="FKBDO[5]"/>
  <ref_port name="FKBDO[6]"/>
  <ref_port name="FKBDO[7]"/>
</swappable_port>
```

PKG-C3

No info. about port swap

PKG-C4

Here is additional preparation

Add swappable info.

Give the constraint from package designer to board designer

Based on the constraint, board designer can change the design

Share the information about constraint and flexibility

=> change of design proposal is possible
LPB Standard Format

Summary
Benefit of LPB format

• Quick & Accurate design/simulation set up
  - No more e-mail/phone call/meetings
  - Avoid human error; eliminate hand edit, version control

• Feedback can be done from any parties, and instantly.
  - For optimization/cost down/quality up feedback

• Easy implementation
  - Human readable, open format XML/Verilog-HDL
  - XML parser available.
  - Simple / light geometry format (G-format:XFL)
Join us!

Visit & Support

• Visit website “LPB format” “LPB forum”
• Please support International Standard IEEE SA P2401

Link Together by LPB standard format