FEC Applications for 25Gb/s Serial Link Systems

Guo Tao, Zhu Shunlin
Guo.tao6@zte.com.cn, zhu.shunlin@zte.com.cn

Asian IBIS Summit, Shanghai, China, November 9, 2015
Agenda

- Introduction
- FEC Applications to Serial Link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary
Introduction

100 Gigabit Ethernet will account for over half of all bandwidth deployed in carrier network in 2014, growing rapidly through 2018.

<table>
<thead>
<tr>
<th>Years</th>
<th>Data Rate (Gb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>10Gb/s</td>
</tr>
<tr>
<td>2013</td>
<td>12.5Gb/s</td>
</tr>
<tr>
<td>2015</td>
<td>25Gb/s</td>
</tr>
<tr>
<td>2018</td>
<td>56Gb/s</td>
</tr>
</tbody>
</table>

IEEE802.3bs/OIF CEI 25G
IEEE802.3bj/OIF CEI 56G
Introduction

Besides equalization techniques, some new techniques have been used for SerDes systems in order to meet 100GE-400GE specs.

Higher Data Rate: 25Gb/s to 56Gb/s

Equalization: De-emphasis+CTLE+DFE

Forward Error Correction: FEC

Fanny Modulation: NRZ or PAM4
Introduction

The Forward Error Correction (FEC) has been used for Increasing serial link system budgets and relaxing BER requirements.

- Code Gain
  Gain vs Higher Frequency

- Time
  Serial Link Latency

- Complexity
  Area and Power
Agenda

- Introduction
- FEC Applications to Serial Link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary
FEC Applications to Serial Link System

FEC Applications on the 100GE standard of IEEE802.3bj

- Backplane System — 100GBASE-KR4
- FEC block is placed between PCS and PMA
- Reed-Solomon Code is suggested, defined in clause 91
- RS(528,514,7) — about 5dB gain
FEC Applications to Serial Link System

Recently adopted FEC
- Fire Code (1604, 1584) – OIF CEI-P
- QC Code (2112, 2080) – 10GBASE-KR
- RS (528, 514, 7) over GF(210) – 100GBASE-KR4
- RS (544, 514, 15) over GF(210) – 100GBASE-KP4
FEC Applications to Serial Link System

FEC Encoding & Decoding diagram
Agenda

- Introduction
- FEC Applications to Serial Link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary
FEC Simulations for 25Gb/s SerDes System

Simulation Setup:

Data rate: 25.78125Gb/s
BER: ~1e-15
Pattern: PRBS 31
Number of bits: 1 million
FEC Simulations for 25Gb/s SerDes System

<table>
<thead>
<tr>
<th></th>
<th>IL/dB</th>
<th>RL/dB</th>
<th>PSXT/dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal</td>
<td>-26.3</td>
<td>-16.8</td>
<td>-47.51</td>
</tr>
</tbody>
</table>
FEC Simulations for 25Gb/s SerDes System

Comparison between with and without FEC

<table>
<thead>
<tr>
<th>AtBER</th>
<th>Nominal Case</th>
<th>Worst Case</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Width/*UI</td>
<td>Height/mV</td>
<td>Width/%*UI</td>
</tr>
<tr>
<td>^1e-12</td>
<td>16.2%</td>
<td>23.1</td>
<td>4.51%</td>
</tr>
<tr>
<td>^1e-15</td>
<td>12.2%</td>
<td>17.4</td>
<td>0.07%</td>
</tr>
<tr>
<td>^1e-17</td>
<td>9.92%</td>
<td>14.2</td>
<td>0.00%</td>
</tr>
<tr>
<td>^1e-12</td>
<td>42.5%</td>
<td>57.0</td>
<td>42.2%</td>
</tr>
<tr>
<td>^1e-15</td>
<td>40.6%</td>
<td>54.8</td>
<td>40.2%</td>
</tr>
<tr>
<td>^1e-17</td>
<td>39.5%</td>
<td>53.4</td>
<td>38.9%</td>
</tr>
</tbody>
</table>

Eye diagram at the BER of 1e-12 of the channel simulation can not meet the requirement of 100GE Standard without FEC. Crosstalk must be concerned in the channel simulation.
# FEC Simulations for 25Gb/s SerDes System

## Comparison between with and without FEC

<table>
<thead>
<tr>
<th>AtBER</th>
<th>Nominal Case</th>
<th>Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Width/*UI</td>
<td>Height/mV</td>
</tr>
<tr>
<td>^1e-5</td>
<td>33.5%</td>
<td>63.6</td>
</tr>
<tr>
<td>^1e-6</td>
<td>29.1%</td>
<td>62.4</td>
</tr>
<tr>
<td>^1e-7</td>
<td>25.9%</td>
<td>61.4</td>
</tr>
<tr>
<td>^1e-12</td>
<td>42.5%</td>
<td>57.0</td>
</tr>
<tr>
<td>^1e-15</td>
<td>40.6%</td>
<td>54.8</td>
</tr>
<tr>
<td>^1e-17</td>
<td>39.5%</td>
<td>53.4</td>
</tr>
</tbody>
</table>

Eye diagram at the BER of 1e-15 of the channel simulation can meet the requirement of 100GE Standard with FEC, while relaxing the BER requirement from 1e-15 to 1e-5 or 1e-6.
Agenda

- Introduction
- FEC Applications to Serial Link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary
A New Proposal for FEC Modeling and Simulation

Current Situation:

- IBIS-AMI model

```
(my_AMIname

(Reserved_Parameters

| Header, such as AMI_version ... |
| Function such as, GetWave_Exists ... |
| Modulation such as, NRZ, PAM4 ... |
| Jitter such as, Dj ... |
| Repeater ... |
```

- EDA Tool
  FEC blocks are not supported in IBIS-AMI model nor in EDA tool

- System Simulation
  Uses the same Serdes IP on the TX and RX end supported by the IC Vendor
A New Proposal for FEC Modeling and Simulation

System vendors strongly expect that IBIS-AMI models can be used for FEC simulations.
A New Proposal for FEC Modeling and Simulation

TX Model *(New Reserved_Parameters)*

RX Model *(New Reserved_Parameters)*

EDA Tool Vendor *(FEC Standards, FEC Settings)*
A New Proposal for FEC Modeling and Simulation

[Reserved_Parameters] / [Model_Specific] → tx_fec / rx_fec ?

On the transmit end
Add the branch ‘tx_fec’ into Model_Specific, then add parameters, config
min/typ/max, mode on/off, such as
(Model_Specific
  (tx_fec
   (config (Usage In)(List "min" "typ" "max") (Type String)
    (Default "typ") (Description "enable fec function setting")
   (mode (Usage In)(Format List "on" "off") (Type String)
    (Default "off") (Description "fec control mode")))

On the receiver end,
Add the branch ‘rx_fec’ into Model_Specific, then add the same parameters
to respond the tx configuration, such as
(Model_Specific
  (rx_fec
   (config (Usage In)(List "min" "typ" "max") (Type String)
    (Default "typ") (Description "enable fec function setting")
   (mode (Usage In)(Format List "on" "off") (Type String)
    (Default "off") (Description "fec control mode"))
Agenda

- Introduction
- FEC Applications to Serial link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary
Summary

- FEC can be used for many dispersion and noise limited systems, such as high-speed serial link systems in order to meet 100GE-400GE specs.
- FEC relaxes PHY BER requirement from 1e-15 to 1e-06 for serial link systems.
- FEC is one of critical techniques for 25-56Gb/s SerDes systems and IBIS-AMI model is an efficient solution for complex IO modeling.
- System vendors strongly expect that IBIS-AMI models can be used for FEC simulations.
- “One model, one platform, one simulator” needed for both passive and active components, such as FFE, DFE, FEC …
Thank you

Tomorrow never waits...