Enabling Full Power-aware Bus Simulation with Non-IBIS Device Model - A Kit using IBIS [External Model]

Skipper Liang
Cadence Design Systems
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Agenda

Introduction

Approach 1: Using IBIS [External Model]

Approach 2: Using an IBIS model to drive the SPICE netlist

Solution: A dummy IBIS model using [External Model] and additional circuit

Summary
Introduction
Bus simulation

- It refers to an automatic process which includes simulation, measurement and report generation against a Bus, especially the memory interface in an EDA tool.
IBIS model

- Intrinsic format - the description of [Pin], [Diff Pin] and [Model Selector]
- IBIS makes Bus simulation possible in an EDA tool
  - easy to assign data groups with individual timing reference
  - Easy to change models and settings in batch mode
SPICE netlist

- Maximum freedom in the circuit format but hard for Bus simulation to be implemented
- Has detailed characteristics of circuits which can’t be fully described by IBIS model
  - Some IC designers prefer using SPICE netlist model than IBIS model
IBIS External Model

- Allow a spice netlist to be called by an IBIS model, which means:

```
[External Model]
Language SPICE

<table>
<thead>
<tr>
<th>Corner</th>
<th>circuit_name (.subckt name)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typ</td>
<td>buffer_typ.spi</td>
</tr>
<tr>
<td>Min</td>
<td>buffer_min.spi</td>
</tr>
<tr>
<td>Max</td>
<td>buffer_max.spi</td>
</tr>
</tbody>
</table>

Parameters - Not supported in SPICE

<table>
<thead>
<tr>
<th>Ports List of port names (in same order as in SPICE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_signal   my_drive my_enable my_receive my_ref</td>
</tr>
<tr>
<td>A_puref A_pdef A_pcref A_gcref A_extref</td>
</tr>
<tr>
<td>D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name</td>
</tr>
<tr>
<td>D_to_A D_drive my_drive my_ref 0.0 3.3 0.5n 0.3n Typ</td>
</tr>
<tr>
<td>D_to_A D_enable my_enable A_gcref 0.0 3.3 0.5n 0.3n Typ</td>
</tr>
<tr>
<td>A_to_D d_port port1 port2 vlow vhigh corner_name</td>
</tr>
<tr>
<td>A_to_D D_receive my_receive my_ref 0.8 2.0 Typ</td>
</tr>
</tbody>
</table>

Note: A_signal might also be used instead of a user-defined interface port
for measurements taken at the die pads
```

- With IBIS format, easy for Bus-Sim to be implemented
- Include detailed characteristics of circuit
SPICE netlist of transistor based device model

- An example of SPICE netlist for a transistor based device model
- For power supply, there are:
  - VDD_Core/Vss_Core
  - VDDIO/VSSIO
  - VREF

Question: if we can use IBIS [External Model] to call this netlist to execute a fully power-aware Bus-Simulation?
Multi-power nets in [External Model] Section?

- Same as a normal IBIS model, an IBIS model with [External Model] can connect to only one PWR / GND pair, usually the VDDIO and VSSIO.

- What will we do for the following:
  1. VDD_Core/Vss_Core
     - A_puref, A_pdref, A_pcref, A_gcref
  2. VDDIO/VSSIO
  3. VREF

[External Model] using SPICE, Verilog-A(MS), or VHDL-A(MS)

[External Model] using SPICE, Verilog-A(MS), or VHDL-A(MS)
Multi-power nets in [External Model] Section? (Cont’)

(spice_io.ckt)

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**•** Except the VDDIO and VSSIO, which will be connected to real power delivery network routing, the other PWR and GND will be connected to a “IDEAL” voltage source.

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**Not Fully Power-Aware**
Approach 2: Using an IBIS model to drive the SPICE netlist
IBIS-drive SPICE netlist

You will have all convenience brought by the IBIS format for Bus-sim

An IBIS model

You will have all connection flexibilities as you use SPICE; For example, all the PWR/GND nodes could be connected to real PDN.

Your System

Your IO SPICE Netlist

VDD_CORE

VDD_IO

VSS_CORE

VSS_IO
An IBIS model

If your IO buffer desires a “1.2V” digital input pattern:

1. This is not a digital signal
2. You will need an IBIS model which output voltage swing is 1.2V
3. Where’s the observation point during Read operation?

Your System

Your IO SPICE Netlist

VDD_CORE VDD_IO

VSS_CORE VSS_IO
Solution: A dummy IBIS model using [External Model] and additional circuits
A simple kit

For “Write”: IBIS which calls a short circuit to pass through digital data using [External Model]

\[ R = 10^{-15} \]

For “Read”: IBIS which calls an open circuit to probe analog received data using [External Model]

\[ R = 10^{15} \]
Write Operation

IBIS which calls a short circuit to pass through digital data using [External Model]

R=1e-15

You will have all connection flexibilities as you use SPICE; For example, all the PWR/GND nodes could be connected to real PDN.
IBIS which calls a short circuit to pass through digital data using [External Model]

R = 1e-15
Write Operation (cont’)

• In a bus simulation, user can easily switch the model of the Controller’s buffer to “Write”
Write Operation (cont’)

Digital data in through IO circuit block
Digital data Directly out
Analog data observed at memory pin

Controller1 SPCI_Wdb pkg_pcb Memory1

Waveform: Voltage (V) vs. Time (ns)
Write Operation (cont’)
For a new project, the kit is re-usable with little modification

Modify according to your new project:

Can almost be re-used through.ibs

Controller1

SPICE_Model

pkg_pcbo

Memory1

VRM
Write Operation (cont’)
For a new project, the kit is re-usable with little modification

Can almost be re-used

through.ibs

Controller1

Modify to the correct voltage level of your IO’s Input node

Modify to the correct voltage level of your IO’s Enable node

21   22   100.00mV  0.85
|===================================================================|= Director System Definition:===================================================================|
| [Model Selector] Dummy_IO |
| Write  single end driver |
| Read   single end Receiver |
|===================================================================|===================================================================|
| Model Write |
|===================================================================|===================================================================|
| [Model] Write |
| Model type 1/0 |
| Polarity     Non-Inverting |
| Enable       Active-High |
| [Voltage Range] 1.500V  1.425V  1.575V |
| [Ramp] |
| variable typ  min  max |
| dV/dt <= 0.120/0.001ns  0.120/0.001ns  0.120/0.001ns |
| dV/dt <= 0.120/0.001ns  0.120/0.001ns  0.120/0.001ns |
| R_load = 50.000 |
| [External Model] |
| Language SPICE |
|===================================================================|===================================================================|
| [Corner corner_name file_name circuit_name (.subckt name)] |
| Corner Typ   write.ckt write |
| Corner Min   write.ckt write |
| Corner Max   write.ckt write |
|===================================================================|===================================================================|
| Ports List of port names (in same order as in SPICE) |
| Ports A_puref A_pdef A_signal my_drive my_enable my_receive |
|===================================================================|===================================================================|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name |
| D_to_A D_drive my_drive A_pdef 0.0 1.2 10p 10p Typ |
| D_to_A D_drive my_drive A_pdef 0.0 1.2 10p 10p Min |
| D_to_A D_enable my_enable A_pdef 0.0 1.2 10p 10p Typ |
| D_to_A D_enable my_enable A_pdef 0.0 1.2 10p 10p Min |
| A_to_D d_port port1 port2 vlow vhigh corner_name |
| A_to_D D_receive my_receive A_pdef 0.0 1.0 Typ |
| A_to_D D_receive my_receive A_pdef 0.0 1.0 Min |
| [End External Model] |
|===================================================================|===================================================================|
| Model Read |
|===================================================================|===================================================================
Read Operation

IBIS which calls a open circuit to probe analog received data using [External Model]

\[ R = 1 \times 10^{15} \]

You will have all connection flexibilities as you use SPICE; For example, all the PWR/GND nodes could be connected to real PDN.
Read Operation (cont’)

IBIS which calls a open circuit to probe analog received data using [External Model]

R=1e+15
Read Operation (cont’)

If you want to observe the waveform before IO:

IBIS which calls an open circuit to probe analog received data using [External Model]

\[ R = 1 \times 10^{15} \]
Read Operation (cont’)

- You will need to modify the netlist of the IO circuit block by adding some “Voltage Controlled Voltage sources” which is controlled by the voltage on IO circuit block’s PAD.

- Connect the dummy controller’s output pad to these “Voltage Controlled Voltage sources”
Read Operation (cont’)

- In a bus simulation, user can easily switch the model of the Controller’s buffer to “Read”
Read Operation (cont’)

IO circuit block through.ibs

Controller1 → SPICE_Model → pkg_pcb → M (Memory1)

Just Overlap
Read Operation (cont’)
For a new project, the kit is re-usable with little modification

Modify according to your new project:

Can be re-used through.ibs

Controller1

SPICE_Model

pkg_pcb

Memory1

VRM
Differential Buffer

No matter true or pseudo, you can use the same kit without any modification because:
(take “write operation” as an example)
Differential Buffer (cont’)
For Truly Differential Buffer type1:

Controller (*through.ibs*)

Because:
1. During load IBIS, you will set dqso0p and dqso0n as TimingRef
2. dqso0p and dqso0n refer to one same model whose polarity is “non-inverting”

EDA tool should or already can *automatically* generate two stimulus signals with 180° phase shift
Differential Buffer (cont’)

For Truly Differential Buffer type2:

Because:
1. During load IBIS, you will set $dqs0p$ and $dqs0n$ as TimingRef
2. $dqs0p$ and $dqs0n$ refer to one same model whose polarity is “non-inverting”

**EDA tool** should or already can **automatically** generate two stimulus signals with 180° phase shift
Because:
1. During load IBIS, you will set dqso\text{p} and dqso\text{n} as TimingRef
2. dqso\text{p} and dqso\text{n} refer to one same model whose polarity is “non-inverting”

EDA tool should or already can **automatically** generate two stimulus signals with 180° phase shift
Because:
1. During load IBIS, you will set dqs0p and dqs0n as TimingRef
2. dqs0p and dqs0n refer to one same model whose polarity is “non-inverting”

**EDA tool** should or already can **automatically** generate two stimulus signals with 180° phase shift
Differential Buffer (cont’)
An example with method2: 3 DQ and 1 pair of DQS
Solution flow chart

New project

Get the kit embedded in this document

Modify “through.ibs” according to your IO’s “input” and “enable” voltage

For “read operation”, observe the waveform…

At the node “out of in”

Just use the kit you’ve modified

At the IO pad

Modify the netlist of IO circuit block by adding some “Voltage Controlled Voltage source” which is controlled by the voltage on IO circuit block’s PAD.
Notes

▪ For analysis of SSN
  – With the full flexibilities as using SPICE, this method allows user to do a power-aware SSN analysis between multiple signals and multiple PDNs, such as VDD_Core/VSS_Core, VDDIO/VSSIO, VTT and VREF together at the same time.

▪ Model modification and change of topology
  – This method requires the change of topology - inserting a Spice block but the wrapping .sp file according to the description in [External Model] is not necessary since it’s ready for use in the kit - easy for re-using this kit in a new project of a new IO.

▪ Read Operation
  – As this method requires the change of topology when building topology, during the analysis of read operation, user will need to modify the netlist of the IO circuit block by adding some “Voltage Controlled Voltage source” which is controlled by the voltage on IO circuit block’s PAD.

▪ Differential Buffer
  – This method can use the same kit without additional modification for both single-end and differential buffer, no matter it’s truly or pseudo.
References

- IBIS specification (v6.1)