Board design and IBIS simulation in consideration of the delay control

Asian IBIS Summit
Tokyo, JAPAN
November 16, 2015

Makoto Matsumuro
IB-ELECTRONICS
Agenda

- Results of the simulation
- Delay only of wiring
- Calculation delay in PKG
- The design which considered package delay
- Problem and future's request
Results of the simulation

The ratio of SI analysis including the High-Speed memory accounts for around 50% every year.
PCB design example for DDR3 interface

SPEC : ±10ps against for DQS.
Skew adjustment control on PCB

SPEC : ±10ps against for DQS.
Calculation : -7.6ps to 8ps for DQS.
Simulation waveform at receiver node

SPEC : ±10ps against for DQS
Calculation : -7.6ps to 8ps
Simulation: -41.5ps to -12.6ps
Skew adjustment analysis including PKG

+ : Progress , - : Delay

**Different**

➢ What is a Factor?
Whole transmission line model of H-S signal

IBIS model includes die capacitance and package-RLC parameters.

IBIS Model

【CHIP + PKG】

High

Low

Driver

Package-LCR

C_comp

IBIS Model

【PCB】

Transmission Line on PCB

extracted by simulator

【CHIP + PKG】

IBIS Model

Packet-LCR

Receiver

Delay in the PKG section compare to PCB?

- Big or small?
- Skew adjustment applies for PKG signals?
## Calculation delay in PKG from IBIS

<table>
<thead>
<tr>
<th>Pin</th>
<th>signal_name</th>
<th>model_name</th>
<th>R_pin</th>
<th>L_pin</th>
<th>C_pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>AU27</td>
<td>DDR_DQS0</td>
<td>DQS</td>
<td>497.40m</td>
<td>6.62nH</td>
<td>2.69pF</td>
</tr>
<tr>
<td>AT27</td>
<td>XDDR_DQS0</td>
<td>DQSN</td>
<td>505.69m</td>
<td>6.22nH</td>
<td>2.63pF</td>
</tr>
<tr>
<td>AP28</td>
<td>DDR_DQ0</td>
<td>DQ</td>
<td>892.42m</td>
<td>5.68nH</td>
<td>1.93pF</td>
</tr>
<tr>
<td>AT28</td>
<td>DDR_DQ1</td>
<td>DQ</td>
<td>964.77m</td>
<td>6.42nH</td>
<td>1.93pF</td>
</tr>
<tr>
<td>AR28</td>
<td>DDR_DQ2</td>
<td>DQ</td>
<td>935.77m</td>
<td>6.14nH</td>
<td>1.89pF</td>
</tr>
<tr>
<td>AN27</td>
<td>DDR_DQ3</td>
<td>DQ</td>
<td>781.75m</td>
<td>5.16nH</td>
<td>1.67pF</td>
</tr>
<tr>
<td>AP26</td>
<td>DDR_DQ4</td>
<td>DQ</td>
<td>798.77m</td>
<td>5.32nH</td>
<td>1.74pF</td>
</tr>
<tr>
<td>AR27</td>
<td>DDR_DQ5</td>
<td>DQ</td>
<td>924.82m</td>
<td>6.04nH</td>
<td>1.86pF</td>
</tr>
</tbody>
</table>

**Model Data**

**Inductance Matrix**
Sparse matrix

<table>
<thead>
<tr>
<th>Row</th>
<th>AU27</th>
<th>6.62nH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AU25</td>
<td>390.56pH</td>
</tr>
</tbody>
</table>

**Capacitance Matrix**
Sparse matrix

<table>
<thead>
<tr>
<th>Row</th>
<th>AU27</th>
<th>2.69pF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AU25</td>
<td>-7.44fF</td>
</tr>
</tbody>
</table>

The delay is calculated as:

\[ T_d = \sqrt{L \cdot C} \]
PKG delay calculation of Controller & Memory

<table>
<thead>
<tr>
<th>Signal</th>
<th>Controller</th>
<th>Memory</th>
<th>Total delay(ps)</th>
<th>Difference with LDQS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L(nH)</td>
<td>C(pF)</td>
<td>delay(ps)</td>
<td></td>
</tr>
<tr>
<td>LDQS</td>
<td>6.62</td>
<td>2.69</td>
<td>133.45</td>
<td></td>
</tr>
<tr>
<td>LDQSn</td>
<td>6.22</td>
<td>2.63</td>
<td>127.90</td>
<td></td>
</tr>
<tr>
<td>DQ0</td>
<td>5.68</td>
<td>1.80</td>
<td>101.11</td>
<td></td>
</tr>
<tr>
<td>DQ1</td>
<td>6.42</td>
<td>1.93</td>
<td>111.31</td>
<td></td>
</tr>
<tr>
<td>DQ2</td>
<td>6.14</td>
<td>1.89</td>
<td>107.72</td>
<td></td>
</tr>
<tr>
<td>DQ3</td>
<td>5.16</td>
<td>1.67</td>
<td>92.83</td>
<td></td>
</tr>
<tr>
<td>DQ4</td>
<td>5.32</td>
<td>1.74</td>
<td>96.21</td>
<td></td>
</tr>
<tr>
<td>DQ5</td>
<td>6.04</td>
<td>1.86</td>
<td>105.99</td>
<td></td>
</tr>
<tr>
<td>DQ6</td>
<td>5.97</td>
<td>1.89</td>
<td>106.22</td>
<td></td>
</tr>
<tr>
<td>DQ7</td>
<td>4.78</td>
<td>1.64</td>
<td>88.54</td>
<td></td>
</tr>
<tr>
<td>LDM</td>
<td>6.95</td>
<td>2.03</td>
<td>118.78</td>
<td></td>
</tr>
</tbody>
</table>

Delay of controller PKG is more than 100ps.

Delay LDQS signal is the biggest.
PCB design considering in skew adjustment

Outer Layer

Inner Layer

Before
The results of delay adjustment in PKG + PCB

Adjust less than ±10ps skew considering PKG + PCB for each byte lane.
**Simulation waveform after skew adjustment**

**SPEC:** ±10ps against for DQS.
**Simulation:** -5.9ps to 5.8ps for DQS.
Using S-parameter for PKG model

S-parameter consider the transmission-characteristic in frequency-domain. But delay time can not be estimated by calculation.
Because it is the model including the package part, a design file can read the receiver side. However, a design file cannot read a package model because the controller side is a S-parameter. Thus, the detailed crosstalk analysis is not possible.
Conclusion

- In the actual PCB layout design such as DDR3 interface, crosstalk noise must be considered both on PKG and PCB. However, to calculate the delay from IBIS RLC model and estimate the optimal trace length on PCB are effective in the early design stage.

- Therefore, propose to add the delay data of HS signals to IBIS model.

- PKG-PCB co-design becomes easy when there is delay data in the S-parameter at header section.

- Hope to EDA tool has a future option that can be extracted delay time from IBIS and S-parameter automatically. Then user can assign a constrained design rule easily to adjust skew!!