DDR4 SI/PI Analysis Using IBIS5.0

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Outline

- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS
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IBIS5.0 can analyze DDR4 SI/PI with high accuracy in a short time!
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DDR3 is replaced by DDR4.

- **Hi-Performance (DDR4)**
  - DDR4 x16 4ch
  - Bandwidth: 4266Mbps

- **Mobile/Commodity (LPDDR4)**
  - LPDDR4 x16 4ch
  - Bandwidth: 3200Mbps
  - DDR4 x64 1ch
  - Bandwidth: 2667Mbps

- **LPDDR2**
  - Bandwidth: 1066Mbps

- **LPDDR3**
  - Bandwidth: 1600Mbps

- **DDR3**
  - Bandwidth: 2133Mbps

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Necessity of IBIS5.0 for DDR4 simulation

IBIS5.0 can analyze SSO noise with high accuracy in a short time.

IBIS5.0:
- SSO accuracy: high
- Simulation Time: short

SPICE Net:
- SSO accuracy: high
- Simulation Time: too long

**DDR4 Timing Budget**

<table>
<thead>
<tr>
<th>Unit Interval [psec]</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td>1066</td>
<td>1333</td>
</tr>
<tr>
<td>1600</td>
<td>1866</td>
<td>2133</td>
</tr>
<tr>
<td>2400</td>
<td>2667</td>
<td></td>
</tr>
</tbody>
</table>

**Decreasing Unit Interval**

Must include SSO noise effect in Package-Board Skew with high accuracy

**Circuit Size vs Simulation Time**

<table>
<thead>
<tr>
<th>Circuit size (SPICE Net)</th>
<th>Analysis TAT (SPICE Net)</th>
<th>Analysis TAT (IBIS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>20000</td>
<td>20000</td>
<td>20000</td>
</tr>
<tr>
<td>40000</td>
<td>40000</td>
<td>40000</td>
</tr>
<tr>
<td>60000</td>
<td>60000</td>
<td>60000</td>
</tr>
<tr>
<td>80000</td>
<td>80000</td>
<td>80000</td>
</tr>
<tr>
<td>100000</td>
<td>100000</td>
<td>100000</td>
</tr>
<tr>
<td>120000</td>
<td>120000</td>
<td>120000</td>
</tr>
</tbody>
</table>

DD2: 200~400 Mbps
DD2: 400~800 Mbps
DD3: 800~2133 Mbps
DD4: 1600~3200 Mbps

Data Rate [Mbps]

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IBIS5.0 issue

We solved the Over Clocking issue in cooperate with EDA developer.

Comparison of the simulation models.

<table>
<thead>
<tr>
<th></th>
<th>SPICE Net</th>
<th>IBIS4.2</th>
<th>IBIS5.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation Time</td>
<td>Longer</td>
<td>Shorter</td>
<td>Shorter</td>
</tr>
<tr>
<td>SSO accuracy</td>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>SI accuracy (~1600Mbps)</td>
<td>High</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>SI accuracy (<del>1866Mbps</del>)</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

High accuracy using IBIS5.0

Over Clocking issue!!!
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Old and new issue
(Over Clocking)

What is the Over Clocking?

IBIS5.0 Simulation (DDR4-2667Mbps)

No 375ps pulses reproduced by Over Clocking.
IBIS Over Clocking mechanism (1/4)

IBIS Low Speed Mode  Pulse Width $\geq$ Initial Delay + Transition Time

Input

Waveform

Output

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IBIS Over Clocking mechanism (2/4)

IBIS High Speed Mode (Over Clocking)

Input

Waveform

Output

Initial Delay prevent switching

Pulse Width < Initial Delay + Transition Time

Endpoint of Falling waveform

Over Clocking
IBIS Over Clocking mechanism (3/4)

IBIS High Speed Mode (Initial Delay Cut)

- **Input**
  - Pulse Width
  - Endpoint of Falling waveform
  - Cut Initial Delay

- **Waveform**
  - Fall
  - Rise

- **Output**
  - Fall
  - Rise

*It is good for IBIS4.2 (w/o SSO noise) ...*
IBIS Over Clocking mechanism (4/4)

IBIS High Speed Mode (IBIS5.0)

Input Pulse Width

Waveform
- Current Changing
- Fall
- Can not cut Initial Delay

Composite Current
- Fall
- Can not use IBIS5.0 at DDR4 ...

Output Traditional Engine
- Fall

Composite Current
- Rise
- Transition
- Time

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Over Clocking modified in the EDA Software

IBIS High Speed Mode (IBIS5.0)

- Pulse Width
  - Move switching point of Fall => Rise

- Over Clocking solved

Input

Waveform

- Fall
- Rise

Output

New Engine

Composite Current

- Fall
- Rise

Composite Current

New Engine

- Fall
- Fall+Rise
- Rise

Pulse Width = Transition Time

IBIS High Speed Mode (IBIS5.0)

- Over Clocking solved

IBIS High Speed Mode (IBIS5.0)

- Over Clocking solved

IBM High Speed Mode (IBIS5.0)

- Over Clocking solved
Over Clocking issue of IBIS5.0 is solved!!

**IBIS5.0 Simulation on New Engine (DDR4-2667Mbps)**

- **Input**
- **750ps**
- **375ps**

- **SDRAM DIE**

**Voltage [V]**
- 1.2
- 1.0
- 0.8
- 0.6
- 0.4
- 0.2
- 0

**Voltage [V]**
- 1.2
- 1.0
- 0.8
- 0.6
- 0.4
- 0.2

**Time [ns]**
- 0
- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10

375ps Pulses reproduced!
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Waveform of the SSO noise: Very Good!!

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<th>CK</th>
<th>Toggle</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/C, CNTL</td>
<td>PRBS7</td>
<td></td>
</tr>
<tr>
<td>DQ</td>
<td>Victim</td>
<td>PRBS7</td>
</tr>
<tr>
<td></td>
<td>Aggressor</td>
<td>PRBS7</td>
</tr>
<tr>
<td>DQS</td>
<td>Victim</td>
<td>Toggle</td>
</tr>
<tr>
<td></td>
<td>Aggressor</td>
<td>PRBS7</td>
</tr>
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</table>

**VDE Voltage waveform (Controller IO)**

- VDE (Controller DIE)
  - VDE\_Max: 1181mV <= SPICE Net
  - VDE\_Min: 1088mV <= SPICE Net
  - VDE\_Max: 1181mV <= IBIS5.0
  - VDE\_Min: 1087mV <= IBIS5.0

- DQ wave (SDRAM DIE)

- Difference in peaks is less than 1mV!!
DDR4 TX DQS-DQ EYE Waveform (@SDRAM DIE)

**DDR4 SI/PI Analysis Using IBIS5.0 (2/3)**

Width of the EYE : Seems Good (see “Expectation for future IBIS”)

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<tr>
<td>DQ</td>
<td>Victim</td>
<td>PRBS7</td>
</tr>
<tr>
<td></td>
<td>Aggressor</td>
<td>PRBS7 (Even/Odd 2pattern)</td>
</tr>
<tr>
<td>DQS</td>
<td>Victim</td>
<td>Toggle</td>
</tr>
<tr>
<td></td>
<td>Aggressor</td>
<td>Toggle</td>
</tr>
</tbody>
</table>

**SPICE Net Model**

EYE Width (min) = 278ps

**IBIS5.0 Model**

EYE Width (min) = 300ps
• Transition Analysis Time: 60ns (one cycle of PRBS7)

Simulation Time: Excellent!!!

Simulation Time [h]

0 50 100 150 200 250

SPICE Net Model

IBIS5.0 Model

Can not use for prototyping

98.6% Reduced!

Better suited for prototyping
(A number of “What-If” analyses in one day)
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**Remaining issue on IBIS5.0**

- IBIS5.0 does not show IO Delay Penalty accurately
  - IBIS5.0 modeling only final-buffer, pre-buffer Delay Penalty can not be considered.

For further simulation accuracy and capability, support of the pre-buffer delay penalty is strongly desired.
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