On-Die Decoupling Model Improvements for IBIS Power Aware Models

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Outline

- IBIS Power-aware modeling overview
- On-die Decoupling models
- Multi-port Decoupling models
- Example Simulations
- Conclusions
IBIS Power-aware Modeling Overview

- Power Integrity modeling uses [Composite Current], [ISSO PU], [ISSO PD] and an IBIS-ISS on-die decoupling circuit model

- Decoupling model external to IBIS currently

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>I_{byp}</td>
<td>Bypass current</td>
</tr>
<tr>
<td>I_{pre}</td>
<td>Pre-Driver current</td>
</tr>
<tr>
<td>I_{cb}</td>
<td>Crow-bar current</td>
</tr>
<tr>
<td>I_{term}</td>
<td>Termination current (optional)</td>
</tr>
<tr>
<td>L_{VDDQ}</td>
<td>On-die inductance of I/O Power</td>
</tr>
<tr>
<td>R_{VDDQ}</td>
<td>On-die resistance of I/O Power</td>
</tr>
<tr>
<td>L_{GND}</td>
<td>On-die inductance of Ground</td>
</tr>
<tr>
<td>R_{GND}</td>
<td>On-die resistance of Ground</td>
</tr>
<tr>
<td>C_{p+b}</td>
<td>Bypass + Parasitic Capacitance</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance for on-die Decap</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent Series Inductance for on-die Decap</td>
</tr>
</tbody>
</table>

* Image from IBIS 6.0 Specification
On-die Decoupling Models

- SPICE model may have pre-driver circuits on separate power supplies
- May be one common ground on-die
- Decoupling model could include VDDQ, VSSQ, VDD, VSS
- What is needed for IBIS to correlate with SPICE?
Multi-port Decoupling Models

- Decoupling circuits may contain proprietary modeling equations or process data

- A non-proprietary model can be an S-parameter or a broadband SPICE macromodel (of the S-parameter characterization)

- S-parameter port options
  - 1-port: VDDQ with VSSQ reference
  - 2-port: VDDQ, VSSQ, with 0 reference
  - 3 or [4] port: VDDQ, VSSQ, VDD, [VSS], with 0 reference
SPICE Setup Examples for Decoupling Model Creation

- Buffer Instance in Hi-Z state:
  - Xbuff ... VDDQ_die VSSQ_die ... Buffer_name

- Port Definition:
  - Single Port
    - P1 VDDQ_die VSSQ_die port=1 Z0=50 DC VDDQ
  - Multi Port
    - P1 VDDQ_die 0 port=1 Z0=50 DC VDDQ
    - P2 VSSQ_die 0 port=2 Z0=50 DC 0

- AC Analysis
  - .lin sparcalc=1 filename='s_model.sNp' format=touchstone dataformat=ma
    freqdigit=10 spardigit=10
  - .ac dec 100 1 10e12
Example Simulation 1 – Ideal VDD  
Comparing Transistor-level and IBIS Model in SPICE

- **L\_VDD = 0** (short)
- **L\_VDDQ = 1.25nH**
- **L\_VSSQ = 1.25nH**
- **L\_PKG = 1.25nH**
1-Port vs. 2-Port Models, I(VSSQ) and I(VDDQ)
V(LOAD) and V(VDDQ_die) - V(VSSQ_die)
Example Simulation 2 – Non-ideal VDD
Comparing Transistor-level and IBIS Model in SPICE

- $L_{VDD} = 1.25\, \text{nH}$
- $L_{VDDQ} = 1.25\, \text{nH}$
- $L_{VSSQ} = 1.25\, \text{nH}$
- $L_{PKG} = 1.25\, \text{nH}$
2-Port vs. 3-Port Models, $I(VSSQ)$ and $I(VDDQ)$
V(LOAD) and V(VDDQ_die)-V(VSSQ_die)
Conclusions

- A 2-port S-parameter (3-terminal macro-model) for on-die decoupling is a better model than a 1-port model for power-aware simulations.
  - This solution requires use of node 0 in the decoupling model.

- Correlating to a SPICE simulation that includes non-ideal supply connections to pre-driver circuits requires extra ports for non-ideal supplies in the decoupling model.

- A multi-port decoupling model is most versatile. Unused ports not connected to a package model should be connected to 0.

- The new IBIS Interconnect BIRD will allow the IBIS-ISS decoupling model to be connected properly to the package model.