IBIS Chair’s Report

Mike LaBonte
Signal Integrity Software
Chair, IBIS Open Forum

Asian IBIS Summit
Taipei, Taiwan
November 14, 2016

http://www.ibis.org/
IBIS Milestones

I/O Buffer Information Specification

- **1993-1994 IBIS 1.0-2.1:**
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- **1997-1999 IBIS 3.0-3.2:**
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- **2002-2006 IBIS 4.0-4.2:**
  - Receiver models
  - AMS languages
- **2007-2012 IBIS 5.0-5.1:**
  - IBIS-AMI SerDes models
  - Power aware
- **2013-2015 IBIS 6.0-6.1:**
  - PAM4 multi-level signaling
  - Power delivery package models

Other Work

- **1995: ANSI/EIA-656**
  - IBIS 2.1
- **1999: ANSI/EIA-656-A**
  - IBIS 3.2
- **2001: IEC 62014-1**
  - IBIS 3.2
- **2003: ICM 1.0**
  - Interconnect Model Specification
- **2006: ANSI/EIA-656-B**
  - IBIS 4.2
- **2009: Touchstone® 2.0**
- **2011: IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

*Touchstone® is a registered trademark of Agilent Technologies, Inc.*
IBIS Version Development

As of 23-Oct-2016

![Bar chart showing IBIS version development from 2 to 7. Each bar represents the number of days from the previous release. The version 7 bar is marked with a question mark.](image-url)
Work In Progress

• Advanced Technology Modeling Task Group
  – IBIS 6.2 dedicated to reference node clarifications
  – Back-channel support (BIRD147.3)
  – C_comp model enhancements
  – Redriver flow enhancements

• Interconnect Task Group
  – External Package/on-die models using IBIS-ISS and Touchstone®

• IBIS Quality Task Group
  – IBISCHK enhancements and documentation
In Progress: IBIS 6.2

- Purpose: Clarify reference terminal conventions in IBIS
- BIRDS submitted, discussed in ATM Task Group
- Editorial Task Group will resume after BIRDS passed
In Progress: Backchannel support

- Purpose: Backchannel to model time domain link training
- BIRD 147.3 recommended by ATM Task Group for acceptance
In Progress: C_comp Model Enhancements

- **Purpose:** Accurate C_comp model supporting frequency and voltage dependence, using IBIS-ISS and Touchstone®
- In ATM Task group, BIRD not yet submitted
In Progress: Redriver Flow Enhancements

- **Purpose**: Provide full redriver channel impulse to Rx Init for optimization, eliminate the need for deconvolution
- **In ATM Task group, BIRD not yet submitted**

$$h_{Rx, in}^{partial} = h_{AC2}$$

$$h_{Rx, in}^{Rx, total} = Rx\text{ Init output} \ast Tx\text{ Init output}$$

$$h_{Rx, out}^{RxNonDFE}$$

$$h_{Rx, out}^{Rx, DFE}$$

(cursors aligned with $$h_{Rx, in}^{partial} \ast h_{RxNonDFE}$$)

$$h_{Rx, out}^{total, RxAll}$$

IBIS Chair’s Report 8
**In Progress: Interconnect BIRD**

- **Purpose:** External Package/on-die models using IBIS-ISS
- **In Interconnect Task Group,** BIRD (draft 42) not yet submitted

---

**Specification Development**

<table>
<thead>
<tr>
<th>Number of terminals</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Pin I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>2 Pin I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>3 Pin I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>4 Pin I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>5 Pin I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>6 Pin_Rail</td>
<td>signal_name</td>
</tr>
<tr>
<td>7 Pin_Rail</td>
<td>signal_name</td>
</tr>
<tr>
<td>8 Buf I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>9 Buf I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>10 Buf I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>11 Buf I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>12 Buf I/O</td>
<td>pin_name</td>
</tr>
<tr>
<td>13 Buf_Rail</td>
<td>signal_name</td>
</tr>
<tr>
<td>14 Buf_Rail</td>
<td>signal_name</td>
</tr>
</tbody>
</table>

[End Interconnect Model]

[End Interconnect Model Set]
In Progress: Approved BIRDs

• All are targeted for IBIS 6.2

<table>
<thead>
<tr>
<th>BIRD</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>179</td>
<td>New IBIS-AMI Reserved Parameter Special_Param_Names</td>
</tr>
<tr>
<td>180</td>
<td>Require Unique Pin Names in [Pin]</td>
</tr>
<tr>
<td>182</td>
<td>POWER and GND [Pin] signal_name as [Pin Mapping] bus_label</td>
</tr>
<tr>
<td>183</td>
<td>[Model Data] Matrix Subparameter Terminology Correction</td>
</tr>
</tbody>
</table>
In Progress: Open BIRDs

- Some are targeted for IBIS 6.2
- Some are superseded by new BIRDs and will be rejected

<table>
<thead>
<tr>
<th>Specification Development</th>
<th>IBIS Chair’s Report</th>
</tr>
</thead>
<tbody>
<tr>
<td>125.1 Make IBIS-ISS Available for IBIS Package Modeling</td>
<td></td>
</tr>
<tr>
<td>145.3 Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword</td>
<td></td>
</tr>
<tr>
<td>157 Parameterize [Driver Schedule]</td>
<td></td>
</tr>
<tr>
<td>158.3 AMI Touchstonefile (R) Analog Buffer Models</td>
<td></td>
</tr>
<tr>
<td>161.1 Supporting Incomplete and Buffer-only [Component] Descriptions</td>
<td></td>
</tr>
<tr>
<td>163 Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]</td>
<td></td>
</tr>
<tr>
<td>164 Allowing Package Models to be defined in [External Circuit]</td>
<td></td>
</tr>
<tr>
<td>165 Parameter Passing Improvements for [External Circuit]s</td>
<td></td>
</tr>
<tr>
<td>166 Resolving problems with Redriver Init Flow</td>
<td></td>
</tr>
<tr>
<td>181 I-V Table Clarifications</td>
<td></td>
</tr>
<tr>
<td>184.1 Model_name and Signal_name Restriction for POWER and GND Pins</td>
<td></td>
</tr>
<tr>
<td>185.1 Section 3 Reserved Word Guideline Update</td>
<td></td>
</tr>
</tbody>
</table>
Days To Resolve BIRDs

As of 23-Oct-2016

Average = 245 days
Most BIRDs Resolved < 9 Months

As of 23-Oct-2016

Number of BIRDs by Months Considered
22 IBIS Members

Organization

Number of Members by Year
Organization

IBIS Officers 2016-2017

Chair: Mike LaBonte, Signal Integrity Software
Vice-Chair: Lance Wang, IO Methodology Inc.
Secretary: Randy Wolff, Micron Technology
Treasurer: Bob Ross, Teraspeed Labs
Librarian: Anders Ekholm, Ericsson
Webmaster: Mike LaBonte, Signal Integrity Software
Postmaster: Curtis Clark, ANSYS
IBIS Meetings

• Teleconferences every week
  – Quality Task Group (Tuesdays)
  – Advanced Technology Modeling Task Group (Tuesdays)
  – Interconnect Task Group (Wednesdays)
  – Editorial Task Group (some Fridays, now suspended)

• IBIS Open Forum teleconference every 3 weeks

• IBIS Summit meetings: DesignCon, SPI, Shanghai, Taipei, Tokyo, EPEPS (2015)
[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.