Agenda

Circuit Simulation

Channel simulation
  LTI system
  Channel simulation

IBIS+AMI model
  What is IBIS+AMI model
  And your concerns?

IBIS+AMI model generation flow – Validation is the KEY!!

Successful Stories:
1. TX – An Output Buffer + FFE
2. RX – An Input Buffer + AGC + CTE
3. A System – TX + Channel + RX

Conclusion
Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
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- Conclusion
• Circuit simulation:

1. **Kirchhoff's current law (KCL)**
   At any node (junction) in an electrical circuit, the sum of current flowing into that node is equal to the sum of currents flowing out of that node.

2. **Kirchhoff's voltage law (KVL)**
   The directed sum of the electrical potential differences (voltage) around any closed network is zero.
Traditional signoff flow –
Using transistor **SPICE netlist** model (con’t)

**Advantages:**
- Accurate PI prediction under **limited** bits transmission
- Accurate jitter prediction under **limited** bits transmission

**Disadvantages:**
- Very slow for SPICE netlist model - Takes weeks/months to get bit error-rate (BER) prediction
- Can’t model the adaptive mechanism in RX

8hr34min for 1024 bit pattern simulation
## Agenda

### Circuit Simulation

### Channel simulation
- LTI system
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### IBIS+AMI model
- What is IBIS+AMI model
- And your concerns?

### IBIS+AMI model generation flow – Validation is the KEY!!

### Successful Stories:
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### Conclusion
LTI – Linear time invariant (con’t.)

• Signal expressed in an impulse-train format:
  
  - Impulse:
    
    \[ \delta(t) = \begin{cases} 
    0, & \text{other than } t = 0 \\
    \infty, & t = 0 
    \end{cases} \]
    
    so, \[ \int_{-\infty}^{\infty} \delta(t)dt = 1 \]
  
  - Quasi-Impulse:
    
    \[ \delta'(t) = \begin{cases} 
    0, & |t| > \frac{\Delta t}{2} \\
    \frac{1}{\Delta t}, & |t| \leq \frac{\Delta t}{2} 
    \end{cases} \]
    
    so, \[ \int_{-\infty}^{\infty} \delta'(t)dt = 1 \]

  - Any Signal:
    
    \[ f(t) = \sum_{n=-\infty}^{\infty} f(n\Delta t)\delta'(t - n\Delta t)\Delta t \]
    
    so, \[ f(t) = \int_{-\infty}^{\infty} f(\tau)\delta(t - \tau)d\tau \]
LTI – Linear time invariant (Con’t.)

- **Linear**
  - System \( x_1(t) \) → System  
  - System \( x_2(t) \) → System  
  - System \( ax_1(t) + bx_2(t) \) → System \( ay_1(t) + b y_2(t) \)

- **Time Invariant**
  - System \( x(t) \) → System  
  - System \( x(t - \tau) \) → System

\[
x(t) = \sum_{n=-\infty}^{\infty} x(n\Delta t) \delta'(t - n\Delta t) \Delta t
\]

\[
x(t) = \int_{-\infty}^{\infty} x(\tau) \delta(t - \tau) d\tau
\]

\[
y(t) = \sum_{n=-\infty}^{\infty} x(n\Delta t) h'(t - n\Delta t) \Delta t
\]

\[
\Delta t \to 0
\]

\[
y(t) = \int_{-\infty}^{\infty} x(\tau) h(t - \tau) d\tau = x(t) * h(t)
\]
Channel-Simulation

- Channel simulation:

\[ \begin{align*}
\text{Input Signal} & \quad \xrightarrow{\text{Convolute}} \quad h(t) \quad \xrightarrow{\text{Convolute}} \quad y(t) \\
X(f) & \quad \xrightarrow{\text{Multiply}} \quad H(f) \quad \xrightarrow{\text{Multiply}} \quad Y(f)
\end{align*} \]

\[ y(t) = \int_{-\infty}^{\infty} x(\tau) h(t-\tau)d\tau \]

*Multi-times faster than circuit simulation!!*
Agenda

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Channel simulation
  LTI system
  Channel simulation

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  And your concerns?

IBIS+AMI model generation flow – Validation is the KEY!!

Successful Stories:
1. TX – An Output Buffer + FFE
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Conclusion
What is IBIS+AMI model (Example: TX)

Accompanied with channel simulator:

- PI prediction with good accuracy without limits on transmission bits
- Jitter prediction with good accuracy without limits on transmission bits
- Very fast for IBIS+AMI netlist model - Takes minutes to get BER prediction
- Can model the adaptive mechanism in RX
What is IBIS+AMI model (Example: TX)

Accompanied with channel simulator:

- PI prediction with good accuracy without limits on transmission bits
- Jitter prediction with good accuracy without limits on transmission bits
- Very fast for IBIS+AMI netlist model - Takes minutes to get BER prediction
- Can model the adaptive mechanism in RX

But you might be concerned:

- Is my system an LTI channel?
- Is my IBIS model accurate enough?
- Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model?
- Is my AMI model accurate enough to describe my EQ?
- Is my Channel Simulator accurate enough to get close to 

![Diagram](Image)
Agenda

Circuit Simulation

Channel simulation
  LTI system
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IBIS+AMI model
  What is IBIS+AMI model
  And your concerns?

IBIS+AMI model generation flow – **Validation** is the **KEY**!!

Successful Stories:
1. TX – An Output Buffer + FFE
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Conclusion
IBIS+AMI model generation flow

Your concern:
- Is my system an LTI channel?
- Is my IBIS model accurate enough? Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model?
- Is my AMI model accurate enough to describe my EQ?
- Is my channel simulator accurate enough to get close to circuit simulator?

Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated.
Validation 1: **Channel Simulation** for

1. Transistor model with EQ on
2. Transistor model with EQ off + AMI model

**Generate AMI model**

**Modified Netlist**

- (Buffer + EQ)
- (Buffer + EQ off)

**SPICE + AMI**

- (Buffer + EQ off) + AMI

Simulation/Comparison via **Channel Sim**

1. (Buffer + EQ) + Test Ckt
2. (Buffer + EQ off) + AMI + Test Ckt

**Match**

**IBIS + AMI model**

**Generate IBIS model**

Simulation/Comparison via **Circuit Sim**

1. (Buffer + EQ off) + Test Ckt
2. IBIS + Test Ckt

**Match**

**Not Match**

**Not Match**

**Not Match**

**Not Match**

**Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated**

**Your concern:**

- Is my system an LTI channel?
- Is my IBIS model accurate enough? Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model?
- Is my AMI model accurate enough to describe my EQ?
- Is my channel simulator accurate enough to get close to circuit simulator?
Validation 1: **Channel Simulation** for

1. Transistor model with EQ on

To qualify the AMI model so generated.

2. Transistor model with EQ off + AMI model
Validation 1: **Channel Simulation** for

1. Transistor model with EQ on
2. Transistor model with EQ off + AMI model

To **qualify the AMI model** so generated.

Why **Channel Simulation**?:
1. AMI model can only be used in **Channel Simulation**
2. Put transistor models under **Channel Simulation** will narrow down the possible cause for any difference happened here to the AMI model so generated.
Validation 2: **Circuit Simulation** for

1. Transistor model with EQ off
2. IBIS model so generated

---

**Your concern:**
- Is my system an LTI channel?
- Is my IBIS model accurate enough? Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model?
- Is my AMI model accurate enough to describe my EQ?
- Is my channel simulator accurate enough to get close to circuit simulator?

---

Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated.
Validation 2: **Circuit Simulation** for

1. Transistor model with EQ off
2. IBIS model so generated

To **qualify the IBIS model so generated**.
Validation 2: **Circuit Simulation** for

1. Transistor model with EQ off
2. IBIS model so generated

To **qualify the IBIS model so generated**.

Define a “mark” and a “target” to tell the quality of the IBIS model so generated

\[
FOM = 100 \cdot \left[ 1 - \frac{\sum_{i=1}^{N} |Y_i(\text{LAB}) - Y_i(\text{IBIS})|}{\Delta Y \cdot N} \right]
\]

\(\Delta Y\): (Max-Min) of Circuit Simulation Waveform

---

**T2B Validation Report**

1. General Information
2. IBIS Correlation Result Summary
3. Simulation Results
   3.1 Model Validation Task 1
Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

Your concern:
- Is my system an LTI channel?
- Is my IBIS model accurate enough? Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model?
- Is my AMI model accurate enough to describe my EQ?
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Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated.
Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**

   - IBIS-AMI model
   - Channel Simulation

2. IBIS-AMI model – **Channel Simulation**

   - AMI Model
     - Pre
     - Main
     - Post

   - Test Fixture

To **qualify the IBIS-AMI model** so generated.
Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
   
   ![Eye Diagram](image)

   (1,024 bits transmitted)

To **qualify the IBIS-AMI model** so generated.

2. IBIS-AMI model – **Channel Simulation**
   
   ![Eye Diagram](image)

   (1e+16 bits transmitted)
Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

To **qualify the IBIS-AMI model** so generated.

![Eye Diagram]

**Also**, to **qualify the Channel Simulator** – if the Channel Simulator behavior close enough to the Circuit Simulator.
Validation 4: **Real Channel** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

Your concern:
- Is my system an LTI channel?
- Is my IBIS model accurate enough? Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model?
- Is my AMI model accurate enough to describe my EQ?
- Is my channel simulator accurate enough to get close to circuit simulator?

Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated.
Validation 4: Real Channel follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

- First of all, check if your system/channel to be analyzed can be treated as LTI or not:
Validation 4: Real Channel follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated
Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. USB 3.0 TX – An Output Buffer + FFE
  2. USB 3.0 RX – An Input Buffer + AGC + CTE
  3. A System – USB 3.0 TX + Channel (PCB+Conn+3m Cable) + USB 3.0 RX
- Conclusion
USB 3.0 TX

**FFE**

- Data_in
- Post[0] Post[1]
- AVSS

**Test Circuit**

- Output Circuit
- Test Circuit

**TX AMI**

- Data_in
- 4 preset taps: P0, P1, P2, P3
- AVSS

<table>
<thead>
<tr>
<th>Eye Contour</th>
<th>Distribution Eye – Circuit Netlist</th>
<th>Distribution Eye – IBIS+AMI model</th>
</tr>
</thead>
<tbody>
<tr>
<td>0dB</td>
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<td>3dB</td>
<td><img src="image3.png" alt="3dB" /></td>
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USB 3.0 TX

**Eye Contour**

<table>
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<th>Distribution Eye – Circuit Netlist</th>
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<tr>
<td>8dB</td>
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<td><img src="image" alt="Distribution Eye 8dB" /></td>
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</table>
USB 3.0 RX

32 levels of strength: P0, P1, P2, ..., P31
# USB 3.0 RX

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<tr>
<td><strong>00100</strong></td>
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<td><strong>01010</strong></td>
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</table>
A System – USB 3.0 TX + Channel + USB 3.0 RX

- Channel Insertion Loss
A System –
USB 3.0 TX + Channel + USB 3.0 RX

- Impulse Response Improvement – By FFE + AGC + CTLE Circuit
A System – USB 3.0 TX + Channel + USB 3.0 RX

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<tr>
<td>TX=3dB</td>
<td><img src="image" alt="TX=3dB Diagram" /></td>
<td><img src="image" alt="IBIS+AMI Diagram" /></td>
</tr>
<tr>
<td>RX=00110</td>
<td><img src="image" alt="RX=00110 Diagram" /></td>
<td><img src="image" alt="IBIS+AMI Diagram" /></td>
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4 preset taps: P0, P1, P2, P3

32 levels of strength: P0, P1, P2, ….P31
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Conclusion
Conclusion

- An accurate IBIS+AMI model could be an alternative approach to validate your “system” design versus a transistor netlist model.

- An accurate IBIS-AMI model consists of two parts – an **accurate IBIS model** and an **accurate AMI model** – **validation** is the key.

- An accurate IBIS should be generated by a tool which can well describe a **truly differential pair** in all V/I, V/T and I/T curves.

- An accurate AMI model should be generated by a tool with a rich library such that the generation tool can use all available means in the library to describe all your possible designs.

- A simulation environment which supports transistor netlist models is fundamental for IBIS+AMI model generation/validation.