Quality checks for power aware IBIS models

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Agenda

- Introduction
- Power aware IBIS 5.1 model simulation
  1. Simulation with sinusoidal noise injected to power rail
  2. Simulation with parasitic of Power and Ground
- Limitation with power aware IBIS 5.1 model
- Proposed solution
- Summary
Introduction

- IBIS 5.1 model is power aware with usage of keywords composite current and ISSO_PU/PD tables
- These keywords take into consideration pre-driver current and gate modulation i.e. driver strength variation due to simultaneously switching noise
- When power aware IBIS model is used in system level simulation power rail is subjected to noise
- IBIS should be sensitive enough to take these variations into account to achieve accurate results
- Quality checks that one should perform and possible solution to correlate with SPICE netlist results are presented
- 28nm-LPDDR4 has been used as a test case
Power Aware IBIS 5.1 model simulation
1st Quality Check: Simulation with sinusoidal noise injected to power rail
Setup to measure the jitter sensitivity
Mismatch in timing jitter

**Case 1:** 100 MHz 200mV p2p sinusoidal noise injected on power rail

100 bits simulated
Data Rate: 2.4 Gbps

IBIS 5.1

Jitter 51 ps

Jitter 101 ps
Mismatch in timing jitter

Case 2: 1 GHz 50mV p2p sinusoidal noise on power rail

100 bits simulated
Data Rate: 2.4 Gbps

IBIS 5.1

SPIKE Netlist

Jitter 26 ps

Jitter 47 ps
2\textsuperscript{nd} Quality Check: Simulation with/without parasitic of power and ground
Case 1: Correlation setup of Power/Ground rail without parasitic

- **Power rail without parasitic**
- **Ground rail without parasitic**
- **R_p**: 0 Ohms
- **L_p**: 0 nH
- **C_p**: 0 pF
- **R_load**: 40 ohms

Diagram:
- Input (In) connected to pad
- Pad connected to R_load (40 ohms)
- R_load connected to Ground rail without parasitic
- Power rail without parasitic connected to pad
PAD waveform when power without any parasitic is used to do correlation with IBIS 5.1

Power with no parasitic

Power of IBIS and SPICE correlate well

FOM is 99.2%
Case 2: Correlation setup of Power/Ground rail with parasitic

- **Rp**: 4 milliohms
- **Lp**: 2 nH
- **Cp**: 3 pF
- **R_load**: 40 ohms

Diagram:

- Power rail with parasitic
- Ground rail with parasitic
- Pad
- **R_load**
With IBIS 5.1 IBIS model

Power waveform

PAD waveform

Power of IBIS and SPICE doesn’t correlate so is the pad voltage

FOM is 93.4%
Limitation with power aware IBIS 5.1
IBIS 5.1 model limitation

- IBIS 5.1 underestimates power supply variation into signal jitter
- IBIS 5.1 correlation with SPICE netlist fails when power/ground rail is subject to parasitic
Proposed solution
Proposed solution for Case1  
IBIS 5.1 with power variation to account for Power Supply Noise Induced Jitter

- Jitter occurs due to change in IO buffer delay and buffer delay is a function of the supply voltage
- In order to model jitter due to power supply. We can use typical, min and max waveforms with only variation in terms of voltage whereas process, temperature remains same and overlap these 3 waveforms to account for PSNIJ
- Variation of +/-5% is accounted from typical voltage of 1.1 V (lpddr4 power supply) to fetch three waveforms and all of them over lapped to generate eye diagram
Improved matching in timing jitter

**Case 1**: 100 MHz 200mV p2p sinusoidal noise on power rail

100 bits simulated

Data Rate: 2.4 Gbps

![Eye Diagram](image)

IBIS 5.1 with typ, min and max overlapped

Jitter 96 ps

Jitter 101 ps

SPICE Netlist
Improved matching in timing jitter

Case 2: 1 GHz 50mV p2p sinusoidal noise on power rail

100 bits simulated
Data Rate: 2.4 Gbps

Jitter 45 ps

IBIS 5.1 with typ, min and max overlapped

Jitter 47 ps

SPICE Netlist
Remarks

- Wherein with new proposed solution one can come close to jitter seen with spice netlist
- To further improve the accuracy more variation in power voltage may be included to account for PSNIJ
Proposed solution for Case 2

- R and C between power and ground have to be explored in order to match impedance between power and ground plane
- Setup with Rc series and C series model added to IBIS 5.1 model

Rp: 4 milliohms
Lp: 2 nH
Cp: 3 pF
R_load: 40 ohms
IBIS 5.1 + Rc series and C series

A model to be calculated in order to match impedance between power and ground
With IBIS 5.1 + [Rc and C series] model

**Power waveform**

![Power waveform graph]

**PAD waveform**

![PAD waveform graph]

**Remark:**

More accurate RC model can be computed using computational algorithms.
Summary
Summary

• Such storage of power voltage variation and storage of delay can be dumped into a file and this file can be used to show the variation of timing jitter by EDA tool
• Series model can be calculated by EDA tool to match the impedance of power and ground