Differential Modeling Flow with Series Model in Verilog-A

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Wei-hsing Huang, SPISim
Wei-hsing.Huang@spisim.com
Sanjeev Gupta, SigIntegrity-Solutions
sanjeev@sigintegrity-solutions.com
Agenda:
• Background & Motivation
• Verilog-A based modeling
  • Differential current
  • External model
• Flow & Validation
• Summary
• Q & A
Background: (1, IBIS CookBook V4)

- Differential buffer: True/Half/Pseudo differential.

- [Diff Pin]: describe differential behavior between two pins.
Method 1 for Half/True differential:

- [Series pin mapping]/Series Model: (2)(3)
Method 2 for Half/True differential:

- **[External Model]:** Spice/VHDL-AMS/Verilog-AMS/IBIS-ISS(4)

Method 1 & 2 can be used together!
Background:

- Data extraction:
  - Common-mode current
  - Differential current
  - $C_{\text{comp}}$ & $C_{\text{diff}}$
Design 1:

I Comm. Mode as PU/PD, PC/GC

A simple “Series R” can describe this particular design

Shifted surface as differential series elem.
Design 2:

Need to describe this surface data in design 2 for V-T extraction
Affect DC steady states (e.g. mismatch)

Options:
- Surface fit in MSE sense:
  - Need to check residue
  - Translate to EFGH elements
- Series MOSFET
  - Or Series current
- Behavioral model?
Design 2 C_diff:

Need to describe this surface data for V-T extraction as well. Affects final transient accuracy.

Options:
- Summarize and add single Series C
- Behavioral model?
Motivations:

● Limitation of “Generic” series model:
  1. Accuracy of transient data for V-T extraction:
    - Inaccurate TR data will pollute waveform...

● Accuracy of transient data for V-T extraction:
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Verilog-A based Diff. current model:

A Verilog-A device can be used in differential V-T extraction.

- Behavioral device is very versatile
- Support operator like ddt, if .. else
- Supports 1/2D look-up table (5), (6)
Verilog-A for V-T extraction:

Simulator only supports 1D table? 2D bi-linear look-up can still be done.

Voltage & freq. Dependent C_Diff (or use cross() to find freq. dynamically)
Completed Series model:

- Verilog-A as external model for model type “Series”
- Verilog-A can work with existing (generic) series model to provide extra accuracy if needed.
Differential modeling flow:

- DC sweep for I-V PU/PD/PC/GC
- AC sweep for C_Comp/C_Diff
- Post-processing to calc DC I_Diff
- Post-processing to calc C_Diff
- Generate table .csv and .va file
- Simulate remaining V-T with diff. I subtracted
Modeling flow validation:

- Use an existing single-ended driver for P and N
- Insert approximate non-linear behavioral R/L/C elements between P and N outputs
- Flow should recreate same PU/PD/PC/GC as driver
- I-V surface plot should reveal inserted resistance
- C_Diff/C_Comp surface should reveal inserted cap
- Correlations of V-T table depends on I_Diff accuracies.
Summary:

- **Verilog-A for differential V-T extraction**
  - Versatile, supports many operators
    - E.g. ddt(Vx), $table_model for 1D/2D lookup
    - Streamlines modeling flow
  - Extract transient differential current
    - Improve V-T extraction accuracies
    - Use Verilog-A to remove rigid series syntax

- **External model for “Series”:**
  - [External model] supports “Series” type model
  - Can work with generic series model
References:

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6. HSpice User’s Manual
Q & A
EDA Expertise in Signal, Power Integrity & Simulation

SPISim is an InSync member.