Verification of PDN Design with Power Aware IBIS MODEL

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Agenda

■ The Present verification methods of Board PDN design and Expectation to Power Aware IBIS Model

■ Challenges for Verification with Power Aware IBIS MODEL

■ Verification with Power Aware IBIS MODEL Summary

■ For the Core power PDN verification
The Present verification methods of Board PDN design and Expectation to Power Aware IBIS Model

- Method1) Apply the Design Guide of IC Maker to the Board design
- Method2) Check with the Target Impedance
- Method3) Compare with the Impedance of Evaluation board of IC Maker
- Method4) Compare with the Impedance of Existing Equipment’s board
- Expectation for Power Aware IBIS Model
Apply the Design Guide to the Board design. The design is good.

Design Guide example

Capacitor conditions:

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>Size</th>
<th>quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1uF</td>
<td>0603</td>
<td>20</td>
</tr>
<tr>
<td>4.7uF</td>
<td>1005</td>
<td>1</td>
</tr>
<tr>
<td>22uF</td>
<td>1608</td>
<td>1</td>
</tr>
</tbody>
</table>

Capacitor

Apply

Board design for the verification
Method2）Check with the Target Impedance

If the PDN Impedance of Board design is lower than the Target Impedance, the design is good.

### IC Datasheet

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Current</td>
<td>Idd</td>
<td>-</td>
<td>-</td>
<td>3000</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>Vdd</td>
<td>1.31 Vdd-3%</td>
<td>1.35</td>
<td>1.39 Vdd+3%</td>
<td>V</td>
</tr>
</tbody>
</table>

**Target Impedance**

\[
Z_{\text{target}} = \frac{V_{\text{dd}} \times 3\%}{I_{\text{dd}} \times 50\%} = \frac{1.35 \times 0.03}{3 \times 0.5} = 0.027\Omega
\]

Frequency range of Target Impedance is uncertain

Board design for the verification
Method 3) Compare with the Impedance of Evaluation board of IC Maker

If the PDN Impedance of Board design is lower than the PDN Impedance of Evaluation board, the design is good.
Method 4) Compare with the Impedance of Existing Equipment’s board

If the PDN Impedance of Board design is lower than the PDN Impedance of Existing Equipment’s board, the design is good.

Design of existing equipment’s board

Board design for the verification

Relative verification
Expectation for Power Aware IBIS Model

Power Aware IBIS (IBIS 5.0) Model Spec.

Power Aware IBIS Model Keywords and relating subparameters
- [Composite Current]
- [ISSO PU]
- [ISSO PD]
- C_comp_pullup
- C_comp_pulldown
- C_comp_power_clamp
- C_comp_gnd_clamp

Source: “IBIS Ver6.1”

Modeling the IO Power current including PDN of the Die

Absolute verification of IO power PDN is enabled
Challenges for Verification with Power Aware IBIS MODEL

- Power Noise Simulation Model
- Power Noise difference between IBIS 4.2 and IBIS 5.0
- Power Noise difference by the Package PDN Model
  IBIS [Define Package Model] (LCR) versus S-param model
- Power Noise difference by the Package Decoupling Capacitor
- Power Noise difference by the Package S-param model frequency range
Power Noise Simulation Model

DDR3L-1600

Controller

Observed “VDD” Voltage Waveform

Observed “DQ” Voltage Waveform

SSO: 32 DQ signals

Our own Model

Package

Mother Board

cap

cap

cap
Power Noise difference between IBIS 4.2 and IBIS 5.0

Controller

IBIS 4.2 or IBIS 5.0

DDR3L

IBIS 4.2 or IBIS 5.0

Package

0.47uFx3

cap

x32

S-param model

Package

Mother Board

cap

cap

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Power Noise difference between IBIS 4.2 and IBIS 5.0

IBIS 5.0 has a larger Power noise.
Power Noise difference between IBIS 4.2 and IBIS 5.0

- In IBIS 5.0, the IO Power current including PDN of the Die is modeled.
- Therefore the accuracy of Power noise simulation is improved.
- Enable to change Board PDN design with Power noise simulation result.
Power Noise difference by the Package PDN Model
IBIS [Define Package Model] (LCR) versus S-param model

Controller

No Capacitor

IBIS 5.0

x32

Capacitor

Package

IBIS [Define Package Model] (LCR) or S-param model

DDR3L

IBIS 5.0

x32

Capacitor

Package

Mother Board
Power Noise difference by the Package PDN Model
IBIS [Define Package Model] (LCR) versus S-param model

We made this model by assuming PKG PDN of IO.

**Package model for IO Power**

**Capacitor**
Capacitor on package: 0.47uF x 3 (0510size, ESL=50pH, ESR=10mΩ)

**C4pad:** VDDx26

**BGApad:** VDDx10

**L1**

**Ln**

**5mm**

10mm

Build-Up

CORE

Build-Up

**Ln view**
Power Noise difference by the Package PDN Model
IBIS [Define Package Model] (LCR) versus S-param model

Making Method Of IBIS [Define Package Model] (L11,C11,R11 for ALL VDD/GND pin)

<table>
<thead>
<tr>
<th>Package model</th>
<th>S-param Extraction</th>
<th>Impedance Analysis</th>
<th>L,C,R Calculation</th>
</tr>
</thead>
</table>

- [Define Package Model] DDR3L_VDDIO
- [Manufacturer] FICT
- [OEM]
- [Description] Controller PKG MODEL for DDR3L SSO Simulation
- [Number of Pins] 100
  - [Pin Numbers]
    - A1 | VDD_1p35
  - [Model Data]
    - [Inductance Matrix] Sparse_Matrix
    - [Capacitance Matrix] Sparse_Matrix
    - [Resistance Matrix] Sparse_Matrix
- [Row] A1
  - A1 | 42e-12
  - A1 | 195e-12
- C=195[pF]
- L=42[pH]
- R=1.7[mΩ]

PDN Impedance BGA short

PDN Impedance BGA open
Power Noise difference by the Package PDN Model
IBIS [Define Package Model] (LCR) versus S-param model

Impedance differences appear at greater than 300MHz in two models.

**Board and PKG PDN Impedance**

<table>
<thead>
<tr>
<th>Impedance [Ω]</th>
<th>Frequency [Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E+02</td>
<td></td>
</tr>
<tr>
<td>1E+03</td>
<td></td>
</tr>
<tr>
<td>1E+04</td>
<td></td>
</tr>
<tr>
<td>1E+05</td>
<td></td>
</tr>
<tr>
<td>1E+06</td>
<td></td>
</tr>
<tr>
<td>1E+07</td>
<td></td>
</tr>
<tr>
<td>1E+08</td>
<td></td>
</tr>
<tr>
<td>1E+09</td>
<td></td>
</tr>
</tbody>
</table>
Power Noise difference by the Package PDN Model
IBIS [Define Package Model] (LCR) versus S-param model

- Impedance differences influence VDD Voltage waveform and DQ Voltage waveform.
- S-param model is higher accuracy than LCR model.

![Graph showing VDD and DQ Voltage waveforms with S-parameter and LCR models compared.]
Power Noise difference by the Package Decoupling Capacitor

Controller

DDR3L

Package

S-param model

IBIS 5.0

0.47uFx3 or No Capacitor

IBIS 5.0

x32

Package

Mother Board
Power Noise difference by the Package Decoupling Capacitor

Impedance differences appear at greater than 10MHz in two cases.

- **0.47uFx3**
- **No capacitor**

![Board and PKG PDN Impedance](chart.png)
- Impedance less than 1GHz is improved by the package decoupling capacitor.
- But the Power noise increase by the package decoupling capacitor.
  (Because the anti-resonance has moved)
- S-param model that we can put capacitors on is necessary to check this result.
- From these simulation results, it is difficult to judge the improvement of the power noise only by impedance.
- It is necessary to check the power noise.
Power Noise difference by the Package S-param model frequency range

Controller

DDR3L

IBIS 5.0

0.47uFx3

x32

S-param model ~1GHz or S-param model ~5GHz

Package

Mother Board

cap

IBIS 5.0

x32

Package

cap
Power Noise difference by the Package S-param model frequency range

A frequency range of S-param model influences the accuracy of the power noise analysis.
Verification with Power Aware IBIS MODEL

Summary
Verification with Power Aware IBIS MODEL

Summary

- In IBIS 5.0, the IO Power current including PDN of the Die is modeled.
- Therefore the accuracy of Power noise simulation is improved.
- Absolute verification of IO power PDN is enabled

- Difference of PKG PDN model format influences VDD Voltage waveform and DQ Voltage waveform.
- S-param model is higher accuracy than LCR model.

- It is necessary for the package mounted with capacitor to model it in S-param.

- The frequency range of the S-param model influences the accuracy of the power noise analysis.

- Expect the spread of IBIS 5.0 and high accuracy PKG PDN model.
For the Core power PDN verification
For the Core power PDN verification

- The currents of the Core power increase lately. Therefore the design verification of Core power PDN of board also is necessary.

package, Die capacitance, Current waveforms are necessary for the high accuracy verification. Also, standardization is expected.
References

  http://www.ibis.org/ver6.1/ for ibis 6.1

- “IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0”, IBIS Open Forum 2011
  http://www.ibis.org/ibis-iss_ver1.0/ for ibis-iss