Embedded DDR4 Design Simulation

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JPCA

- Japan Electronics Packaging and Circuit Association

JPCA Electronics Related Industry

- Material
- Chemical
- Circuit
- Equipment • Test
- Trading • Service
Japanese PCB Design/Manufacturing

**Past Japanese Development**

- **System Developer**
  - Architecture Design
  - Schematic
  - PCB Layout Design
  - Manufacturing

**Selection and Concentration**

**Current Japanese Development**

- **System Developer**
  - Architecture Design
  - Schematic

- **Management/Control**

- **Outsource**
  - PCB Layout
    - Global EMSs Taiwan, China
  - Japanese EMSs ....

- **Past Japanese Development**

- **Current Japanese Development**
Who Is Concerned about Design Rules?

**System Developer**
- High Speed Circuit Design
- Many people needed to satisfy difficult issues
- Difficult to satisfy all

**PCB Design/Manufacturing Related Issues**
- Via design
- Line/Space
- Layer Stack-up
- PCB Material
- Line width
- Standard, Specification
- Skew
- Jitter
- Power Integrity
- Signal Integrity
- On Die Terminator
- I/F Topology

System Developer:
Please refer IC’s PCB Design Guide (^-^;)
And so on, give me simulation report

Consignment All
Design Bureau

We have to correct all information and check all by ourselves...
JPCA Design Academy

- Found JPCA Design Academy
  - PCB Design Review
  - High-Speed Design Guideline
  - Design/Simulation Consulting
  - Simulation Tools
  - Simulation Engineer Training
  - Transfer Technical Documentations in Japanese

Leave It to Me!!

I Received order but...... It is Too difficult
DDR4 Design Project

- JPCA Design Academy’s Project

ASIC Vender’s Reference Design

User’s Requirements

- Material FR4
- Line / Space
- Via size
- Cross Section

Change Layout

Cannot Apply the Same Design

Change Condition

Propose!

Reference Design
- Megtron 6
- 16 Layers
- Constraint

* Satisfy the Manufacturing Requirements
* Satisfy the System Developer’s Requirements
DDR4 Design Project

• Step 1: 2015
  – ASIC Vendor’s Reference Design
    • Review the JEDEC DDR4 Specification
    • Review the Reference Board Rule/Topology
    • PI/SI Simulation
    • Measurement
    • Release the DDR4 Design Guide
DDR4 Design Project

• Step 2: 2016
  – 3 Japanese PCB Manufacturers Design Board (Case1, Case2, Case3)
  – Use JPCA Design Academy’s DDR4 Design Library (Guide)
    • 3 Different Stackup
    • 3 Different Design
    • Use the Same Schematic
    • Use the Same Design Guide
    • Now on going Design, Simulation
    • Will Measure
    • Will Release Design Guide Rev. 2
Step 2

JPCA Design Academy

1. DDR4 System Structure
2. Basic Topology, Design Rule, , ,
3. Basic PCB’s Design Guide (Via, Stackup, , ,)
4. SI Simulation Sample/Methodology
5. PI Simulation Sample/Methodology

DDR4 Library

PCB Manufacturer A

A’s PCB Parameter

Optimized Library

PCB Manufacturer B

B’s PCB Parameter

Optimized Library

PCB Manufacturer C

C’s PCB Parameter

Optimized Library
DDR4 Design Project

• Step 3: 2017~
  – Driver DDR4 Design Guide Rev.2
  – Design Consulting
  – Simulation Consulting

• Challenge New Technology (New Project)?
Trial Boards
Reference Board

Topology of DQ

Controller (ASIC)

ODT (Pull-up)

Write

Read

ODT (Pull-Up)

DDR4
Case1: 10 Layers/Buildup (4-2-4/IVH)
Case2: 8 Layers/Through
Case3: Buildup 10 Layers (4-2-4)
Case1: Trial Board
Top

DDR4 x 4
U60, U61, U62, U62

Kintex UltraScale
U1
DDR4 all Signal

DDR4 Memory x 4
16bit x 4 = 64bit

Kintex UltraScale Controller
Address Lines
Address Topology

U1 Kintex

DDR4 mem1

DDR4 mem2

DDR4 mem3

DDR4 mem4
Sample of Package Delay table is shown as above
- longest is 31.889mm
- Shortest is 11.529
- Diff: 20.36mm = 135.8ps (6.67ps/mm)

It’s required to include PKG routing length at
- board layout stage (matched timing)
- IO selecting stage using SI simulation (skew investigation)
Address 0

Ideal Plane
at U60, U61, U62, U63

Plane model  ON
On Die model  Off
Pkg model     Off

Address 10 at U63
On Die model  ON
Pkg model     Off
Address: On Die & Pkg model

On Die model  Off

Pkg model  Off

On Die model  ON

Pkg model  ON
Address, Clock and Power

PKG model  ON
Die model   Off
DQ Lines
DQ0 Topology

Kintex (U1) to DDR4 Mem (U60) via VIA22 and VIA220.

- L1(TL_53): 0.74 mm, 40.531 Ω
- L1(TL_50): 0.57 mm, 31.879 Ω
- L5(TL_52): 22.98 mm, 41.912 Ω
- L5(TL_51): 28.57 mm, 34.856 Ω
- L5(TL_54): 11.43 mm, 41.912 Ω

Write mode and Read mode transitions through ODT (On-die termination)
Simulation Results (DQ0-7, DM0)

Package model Off (PCB delay only)

Package model ON (Pkg skew should be added to PCB delay)
Different DQ0 Results Depend on IBIS Models

U60

On-Die model ON
Pkg model Off
DQ: Die/Pkg Model

Power
Red: Die/Pkg model Off
Blue: Die/Pkg model ON

DQ(DQ0-8) Die/Pkg model ON (Very Stable Power)
Bottom: Differential Signals

Red: Clock Line
Pink: DQS
DQS Topology

All Differential Signals are broken out from Top Layer to Bottom Layer.
Clock, DQS

On-Die model ON
Pkg model Off

Voltage (V)

Time

Voltage (V)

Time (ms)
Z Impedance

VDD1.2V DDR4 Power Plane
Coupling or Skew Analysis?

Package length is required to add to:

1. PCB matched length routing
2. Pkg Skew investigation
3. Pkg model with coupling effect + Pkg delay simulation
Required Specification

• Pkg signal coupling simulation with Pkg skew effect is required for recent DDR4 bus simulation

• Current IBIS model:
  – Length could be added in to [Pin Numbers] section
  – Coupling model could be specified in [Define Package Model] section
  ➢ But both coupling with length effect couldn’t be allowed at one simulation.
  ➢ Length should be specified in [Define Package Model]
    ➢ [Length Matrix] Sparse_Matrix
      [Row] A1
      A1  8.7e-11  (unit Second)