Signal Integrity Analysis for 56G-PAM4 Channel of 400G Switch

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Celestica
Agenda

• Background
• 200GBASE-KR4
• 400GAUI-8 C2M/200GBASE-CR4
• CEI-56G-VSR-PAM4
• Conclusion
Background

- Celestica focuses on advanced switches, storage and server.
- The switch bandwidth is moving from 100G to 400G.
- Data rate is moving from 25 Gbps to 56 Gbps.
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- Conclusion
• This channel is between switch chip and PHY chip.

• Megtron 4 level material is used for the analysis.
The simulation results are shown above. The channel includes an 11 inch trace on the Switch Card, a 7 inch trace on the I/O Card and one connector. The channel can meet the 200GBASE-KR4 specifications of the passive channel requirements.
200GBASE-KR4- COM Simulation

• Consideration of the 9 FEXT and 8 NEXT crosstalk models to run the COM.
• The crosstalk considers the crosstalk in BGA area and the crosstalk in connector area.

Simulation results show that the 11 inch trace in Switch Card and 7 inch trace in I/O Card can pass the COM specification with default package model.
The simulation settings and results are shown in the Table and Figure below. The channel is from switch chip to PHY chip.

<table>
<thead>
<tr>
<th>Trace Length</th>
<th>PVT Corner: Best</th>
<th>PVT Corner: Typical</th>
<th>PVT Corner: Worst</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Eye Width/Eye Height @BER=1e-6 in Sim</td>
<td>Eye Width/Eye Height @BER=1e-6 in Sim</td>
<td>Eye Width/Eye Height @BER=1e-6 in Sim</td>
</tr>
<tr>
<td>11inches in Switch Card and 7inches in I/O Card</td>
<td>4.52ps/96mV</td>
<td>4.33ps/95mV</td>
<td>4.33ps/141mV</td>
</tr>
<tr>
<td></td>
<td>4.71ps/142mV</td>
<td>4.71ps/141mV</td>
<td>4.71ps/141mV</td>
</tr>
<tr>
<td></td>
<td>4.52ps/91mV</td>
<td>4.52ps/90mV</td>
<td>4.52ps/90mV</td>
</tr>
</tbody>
</table>

Simulation results show that the channel including total 18 inches of trace can support 53.125 Gbps data rate.
The simulation settings and results are shown in the Table and Figure below. The channel is from the PHY chip to switch chip.

<table>
<thead>
<tr>
<th>Trace Length</th>
<th>PVT Corner: Worst Eye Width/Eye Height @BER=1e-4 in Sim</th>
</tr>
</thead>
<tbody>
<tr>
<td>11 inches in Switch Card and 7 inches in I/O Card</td>
<td>2.64ps/5mV</td>
</tr>
<tr>
<td></td>
<td>2.64ps/14mV</td>
</tr>
<tr>
<td></td>
<td>2.45ps/5mV</td>
</tr>
</tbody>
</table>

There is some issues with the time domain simulation of PHY TX and switch chip RX. Celestica is working with the chip vendor.
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The 400GAUI-8 C2M specification has defined the requirement from the host transmit to the test fixture. The topology is shown in the Figure below. Megtron 7 PCB material has been used in this channel.
Simulation results show that the channel, including 11.4 inches of trace, can meet the 400GAUI-8 C2M specification passive requirements.
The copper cable loopback channel topology with 200GBASE-CR4 is shown below.

• Simulation results show the IL/RL of two 11.4 inch channels with a 2.5m 28AWG cable loop back can meet the 200GBASE-CR4 specification passive requirements.
Simulation results show the IL/RL of two 11.4 inch channels with 3m 28AWG cable loop back can meet the 200GBASE-CR4 specification passive requirements.
The channel margin shall be greater than or equal to 3dB after COM calculation for 200GBASE-CR4 Channel.

9 aggressor FEXT channels and 8 aggressor NEXT channels on both side of the victim channel are considered for the COM crosstalk analysis. The major contributors to crosstalk such as traces, vias, cable paddle card are considered for the crosstalk modeling. The detailed trace modeling with crosstalk is shown below.

Simulation results show that the channel including two 11.4 inch traces with 3m 28AWG QSFP-DD cable assembly, Case1 can pass and Case2 cannot meet the IEEE802.3cd Specification COM requirement for 200GBASE-CR4 based on the default package S parameters.
Simulation results show that the channel including two 11.4 inch traces with the 2.5m 28AWG QSFP-DD cable assembly, can meet the IEEE802.3cd/D2.2 Specification COM requirement for 200GBASE-CR4 based on the default package S parameters for both cases.
Simulation results show that the channel including two 11.4 inch traces can support the 3m 28AWG QSFP-DD cable for 53.125G rate.
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The CEI-56G-PAM4-VSR specification defines the requirement from the host transmit to the external IO connector. The topology is shown in the Figure below. Megtron 7 PCB material has been used in this channel. Note that from Host PCB to Connector insertion loss is up to 8.5 dB.
Simulation results show that the channel including an 11.4 inch trace with one connector can meet the passive requirement of the CEI-56G-VSR-PAM4 specifications.
• The simulation results are shown in the table below.

<table>
<thead>
<tr>
<th>Trace Length</th>
<th>Eye Width/Eye Height (@BER=1e-6 in Sim)</th>
<th>Eye Width/ Eye Height (@BER=1e-6 in spec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.4 inches</td>
<td>11.48ps/51mV</td>
<td>&gt;=8.28ps/35 mV</td>
</tr>
<tr>
<td></td>
<td>11.11ps/52mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12.05ps/51mV</td>
<td></td>
</tr>
</tbody>
</table>

• Simulation results show that the channel including a 11.4 inch trace with one connector can meet the eye height requirement of the CEI-56G-VSR-PAM4 specification at TP1a.
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