DDR System Simulation: What Issue to Simulate

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KEI Systems
# JEDEC DDR Specifications

<table>
<thead>
<tr>
<th></th>
<th>DDR</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR3L</th>
<th>DDR3U</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5</td>
<td>1.35</td>
<td>1.25</td>
<td>1.2(IO) + 2.5(Core)</td>
</tr>
<tr>
<td>ODT (ohm)</td>
<td>N/A</td>
<td>50/75/150/OFF</td>
<td>20/30/40/60/120/OFF</td>
<td>34/40/48/60/80/120/240/OFF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diff Clock</td>
<td>Single</td>
<td>Diff</td>
<td>Diff</td>
<td></td>
<td></td>
<td>Diff</td>
</tr>
<tr>
<td>DQS</td>
<td>Single</td>
<td>Single/Diff</td>
<td>Diff</td>
<td></td>
<td></td>
<td>Diff</td>
</tr>
<tr>
<td>Driver Z (ohm)</td>
<td>Full/Half</td>
<td>Full/Reduce</td>
<td>34/40</td>
<td></td>
<td>34/40/48</td>
<td></td>
</tr>
<tr>
<td>ADD/CMD Topology</td>
<td>T</td>
<td>T</td>
<td>Fly-by</td>
<td>Fly-by</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory Size</td>
<td>~64Mbit</td>
<td>~4GBit</td>
<td>0.5~8GBit</td>
<td>2/4/8/16GBit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DQ Prefetch</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td></td>
<td>8X2 (4x4)</td>
<td></td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>100~200</td>
<td>200~400</td>
<td>400~1066</td>
<td>800~1600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Speed (Mbps)</td>
<td>200~400</td>
<td>400~800</td>
<td>800~2133</td>
<td>1600~3200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus Width (Max)</td>
<td>4/8/16/32</td>
<td>4/8/16</td>
<td>4/8/16</td>
<td>4/8/16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
New Feature of DDR2

• ODT (DQ/DQn)
  • 50/75/150/OFF
  • Terminate to Vtt (Vdd/2)

• Output Characteristics
  • Full Strength/Reduced Strength

• Diff Clock/ Diff DQ

Technical Diagrams:
- ODT configurations
- Output characteristics
- Diff Clock/Diff DQ waveforms
**DDR2**

- **Topology (Clock/Add/CMD/CTRL)**
  - Equal Delay
  - Terminate to Vtt (Vdd/2)
**DDR2 Simulation**

- Select best combination Driver and Receiver (ODT)
  - Full Strength/Reduced Strength ↔ 50/75/150 ohm
  - 6 Combinations
- Topology (Clock/Add/CMD/CTRL)
  - Equal Delay
  - Termination
  - Place
  - Value
Combination Driver and Receiver

- Timing
  - Driver: Low/Receiver: High
    - High Signal Level, Fast, Shoot
    - High Power, Noisy (SSN, EMI)
  - Driver: Low/Receiver: High
    - High Signal Level, Fast, Shoot
- Driver: 34/40 ohm
- ODT: 50/75/150 ohm
DDR2/DDR3 Timing Simulation

- Derating
  - Specification Assign on Vref Timing
  - IC Works on Threshold Voltage
  - Necessary to adjust the timing on Vref to Threshold Voltage
- Specification based on 1v/ns signal
DDR3

- ODT
  - 20/30/40/60/120/OFF
- Output Characteristics
  - Full Strength/Reduced Strength
- Fly–by Topology (Clock/Add/CMD/CTRL)
  - Daisy–Cain with Short Stub
  - Terminate to Vtt (Vdd/2)
Simulation of DDR3 System

• Select best combination Driver and Receiver (ODT)
  • Full Strength/Reduced Strength – 20/30/40/60/120 ohm
  • 10 Combinations

• Fly-by
  • Effect of Stub Length
  • Leveraging
    • Read (Max. Timing Skew form 1\textsuperscript{st} DDR to Last DDR) – Fly-by
    • Write (Option)

Hold Margin is Small

⇒ CK Phase shift

Setup/Hold Margin are Proper

KEI Systems
DDR4 Features

- Faster (Two times faster than DDR3)
  - DDR3: 400MHz ~ 800MHz, 933, 1066 MHz
  - DDR4: 800MHz ~ 1600MHz (2400, 2666)
  - 2.5V Core Logic

- Lower Power
  - More ODT Value
  - Partial Refresh (LPDDR technology)
  - 1.2V Interface
  - POD Termination
  - DBI (Data Bus Inversion)
DDR4 Technology

- Same Technology of DDR3
  - ODT (34/40/48/60/80/120/240)
  - Fly by Wire
  - Output Impedance (34/40)

- New Feature
  - Multi-Purpose Register (MPR)

POD (Pseudo Open Drain) makes simulation difficult
• ODT Termination Voltage: Vtt (DDR2/DDR3)

• POD (ODT Termination Voltage: Vdd (DDR4))

• POD Moves Vref
DBI (Data Bus Inversion)

- POD Termination
  - Low Level Data Drive High Current/High Level Data Drive no Current
  - When Low Level bits are Majority, Invert the Data
  - In Any Data, High bits are Majority
  - Simultaneous Switching: Less than 4 bits
    - Lower SSN

![Diagram showing DBI and I/O Cell MUX for cases with less than or equal to 4 zeroes and more than 4 zeroes]
DDR4 System Design/Simulation

- DDR3 Methodology Can not be Used for DDR4 Design/Simulation
  - Too Many combination of Driver–Receiver (18 Ways)
    - ODT: 34/40/48/60/120/240
    - Ron: 34/40/48
  - Vref Voltage is not fixed
- Vref, DQ Training
- ZQ Calibration
MPR (Multipurpose Register)

- Implement from DDR3
- Strongly Enhanced on DDR4
  - 4 4 Byte Registers
  - Training
• Set/Idle State and Read/Write State
  • Initial
    • Initialize
    • ZQ Calibration
  • Set/Idle State
    • Write Leveling
    • ZQ Calibration
  • Refreshing
  • Read/Write State
Adapt Eye Mask

- Vref is Unstable
- Can’t Fix Vref Based Timing Specification (DDR3)
  - No More Derating

### DRAM Data Timing

<table>
<thead>
<tr>
<th>DRAM Data Timing</th>
<th>tDQSq</th>
<th>tDQH</th>
<th>tDQHc</th>
</tr>
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<tbody>
<tr>
<td>DQS_t delay</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DQS_c delay</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Rx Mask Diagram

- DQS, DQS Data-in at DRAM ball
- Non Minimum Data-Eye / Maximum Rx Mask

- DQx
- VddW TOTAL

KEI Systems
DDR4 Simulation is very difficult

- Timing Analysis for Training
  - ZQ Calibration
  - Vref Training
  - Write Leveling
- SSN becomes more important
  - Lower voltage (1.2V)
  - Faster signal (dv/dt)
- X’talk
  - Faster signal (dv/dt)
- Package Model
  - Signal skew of In Package connection
  - In package X’talk (Bigger than on board connection)
  - Stub for Fly–by
IBIS Model for DDR4 Simulation

- Power Aware (IBIS 5.0)
- Vref Training/Write Leveling
  - Eye Mask
- Overclock
- Support DQ Training
  - How to determine best Driver–Receiver simulation model
- Fly–by Support
  - In–Package Stub
DDR5

• JEDEC Already working DDR5 Specification
  • Focus in 2018
    • Products in 2020?
  • x2 Faster than DDR4
  • DFE (Decision Feedback Equalizer)
    • Reduce ISI
  • More Training
  • Bigger Memory size
  • Power Reduce Technology
    • Analog Filter? (to reduce ISI jitter)

• Hard to Simulate
Conclusion

- DDR2 System Simulation
  - ADD/CMD/CTRL Topology
  - Combination of Driver/ODT
  - Sign-off Analysis
- DDR3 System Simulation
  - ADD/CMD/CTRL Fly-by Topology
  - Combination of Driver/ODT
  - Sign-off Analysis
- DDR4 System Simulation
  - ADD/CMD/CTRL Fly-by Topology (in Package Etch)
  - Combination of Driver/ODT (Too many combination to Simulate)
  - Can’t execute Sign-off Analysis (Can’t follow Training Result)
  - Power aware/Over Clock
- DDR5 System Simulation?
  - More Intelligent I/F specification (More training functions)
  - Analog Filter Circuit? (IBIS AMI?)