Interconnect Modeling Update
Using IBIS-ISS and Touchstone

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Agenda

- History
- The need for improved interconnect support
- Principles of the Interconnect Proposal
  - Structure
  - Terminals, Models and Sets, and Groups (new)
  - New Keywords
- An example explained
- New or changed features
- Summary
History

- Interconnect Task Group resumed meeting in early 2014
  - Received draft BIRD from Walter Katz (SiSoft) to support IBIS-ISS packages within IBIS

- BIRD189.x uploaded (awaiting approval)
  - [http://www.ibis.org/birds/](http://www.ibis.org/birds/)
  - 41 pages with examples
  - Still resolving some issues
  - Comments welcome

- Intended for IBIS Version 7.0

- **Brief** overview with some key points is given here
Why Update Interconnect Modeling?

- Improve package models with IBIS-ISS (an HSPICE subset) and Touchstone support

- Package modeling in IBIS stable since 2000
  - [Pin], [Package], [Package Model]
  - [Alternate Package Models] selector added
  - Limited support of loss, crosstalk and/or partitioning

- EBD (Electrical Board Description) for boards; No coupling and limited package model application

- IBIS, IBIS-ISS, Touchstone 2.0 and ICM are separate specifications
  - Limited interaction between them for package modeling
  - ICM (Interconnect Model) never adopted by industry
Features of the Interconnect Proposal

- Supports...
  - IBIS-ISS and Touchstone models (common in industry)
  - Both I/O and supply (POWER and GND) connections
  - (New) optional Die pad interface between Pins and Buffers
  - I/O pin_names as terminal qualifiers
    - May have optional Aggressor_Only designation
  - POWER and GND terminal qualifiers by pin_name, pad_name, signal_name or [Pin Mapping] bus_label for rail connections with direct or combined terminals
  - Many other features not covered here

A few objectives for the Interconnect Modeling proposal
Structure of the Interconnect Proposal

[Model] buffer definition but with explicitly identified terminals

NEW!

Introduces optional Die pad interface for terminals separate from Buffer and Pin interface terminals

1 VCC_5.0 POWER
2 VCC_3.3 POWER
3 DATA1 DATA_MODEL
4 VSS GND
5 VCC_5.0 POWER
6 VCC_3.3 POWER
7 DATA2 DATA_MODEL
8 VSS GND

pin_names, signal_names, and model_names from the [Pin] keyword

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Relates to Physical Structures

One-to-one path connection; Die pad interface optional; Aggressor_Only designation optional
Terminals at Buffer, Die Pad and Pin Interfaces

Original IBIS (4.0 and earlier)
• Pins are explicit
• Buffer terminals implicit in [Model]
• Die pad terminals same as buffer terminals
• Packages defined connections between pins and buffers

Current Proposal
• Die pad terminals are now explicit
• Buffer terminals are now explicit
• [Pin]s are…. still pins
• Separate interconnect definitions can be created between …
  • Pin-to-Die pad terminals,
  • Die pad-to-Buffer terminals,
  • Pin-to-Buffer terminals (still) supported
Physical Rails (Can be Merged)
New Keywords and Subparameters (Limited Discussion Here)

- [Bus Labels] | bus_label
- [Die Supply Pads] | pad_name, optional bus_label
- [Interconnect Model]/[End Interconnect Model]
  - Unused_port_termination <Open | Ref.| Unused port ref. Z
  - Param | parameter passing
  - File_IBIS-ISS | names IBIS-ISS file
  - File_TS, File_TS0 | names Tstone file
  - Number_of_terminals=<value> | number of terminals
  - <terminal lines> | described later

- [Interconnect Model Set]/[End Interconnect Model Set]
- [Interconnect Model Set Group]/[End Interconnect Model Set Group] (New and changed from “Selector”)

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Interconnect Hierarchy

[Interconnect Model Group] Group 1

[Interconnect Model Set] Set1

[Interconnect Model] ICM1a

[Interconnect Model] ICM1b

[Interconnect Model Group] Group 2

[Interconnect Model Set] Set2

[Interconnect Model] ICM2a

[Interconnect Model] ICM2b

[Interconnect Model Set] Set2

[Interconnect Model] ICM2a

[Interconnect Model] ICM2b
[Interconnect Model Set]s
[Interconnect Model Set Group]s (New)

- [Interconnect Model Set] <set_name>
  - Encapsulates one or more Interconnect Models

- [Interconnect Model Set Group] <group_name>
  - References one or more Interconnect Model Sets to be used together
  - Should be used to establish a complete path for selected buffers
  - <group_name> helps in identify the buffers that are selected for simulation

Some Example Groupings and Applications
  - Separate groups: one per interface (e.g., memory, network)
  - Separate groups for coupled vs. single-line simulations
  - Different sets for different power delivery network complexities
    - POWER connected at single pin, single buffer terminal
    - POWER connected through multiple pins, rails to individual buffer terminals
[Interconnect Model]

- [Interconnect Model] <interconnect_model_name>
  - Connections between terminals with IBIS-ISS or Touchstone files
  - Terminal connection points at Buffer, Die pad, or Pin interfaces
  - Identifies rail or I/O terminals
  - Allows pin_name, signal_name, pad_name, or bus_label terminal qualifiers for rails (and pin_name for I/O terminals)
  - Identifies whether a coupled signal is only an aggressor or also “experiences” coupling from other sources

How package and on-die electrical information is generated and delivered today
<Terminal lines> Syntax

- All column entries on one line:

  <Terminal_number> <Terminal_type>
  <Terminal_type_qualifier> <Qualifier_entry>
  [Aggressor_Only]

- <Terminal_number> is IBIS-ISS node position or Touchstone port number

- Allowable <Terminal_type> names and associations next
## Allowable `<Terminal_type>` Associations

<table>
<thead>
<tr>
<th><code>&lt;Terminal_number&gt;</code></th>
<th><code>&lt;Terminal_type&gt;</code></th>
<th><code>&lt;Terminal_type_qualifier&gt;</code></th>
<th><code>&lt;Qualifier_entry&gt;</code></th>
<th><code>&lt;Aggressor_Only&gt;</code></th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin_I/O</td>
<td>X</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Pad_I/O</td>
<td>X</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Buffer_I/O</td>
<td>X</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Pin_Rail</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>Pad_Rail</td>
<td></td>
<td></td>
<td></td>
<td>Z</td>
</tr>
<tr>
<td>Buffer_Rail</td>
<td></td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>Pullup_ref</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulldown_ref</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power_clamp_ref</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gnd_clamp_ref</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ext_ref</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

`<Qualifier_entry>`: "X" I/O pin_name; "Y," or "Z": POWER or GND name. Optional "A": "Aggressor_Only"
Example Showing Connections

Buffer Terminals

Die Pad Terminals

Pins

C1 VDD  POWER
A1 DQ1  DATA_MODEL
C2 VSS  GND
A2 DQ2  DATA_MODEL

VDDQ
VSSQ
The [Die Supply Pads] keyword establishes pad_name <Qualifier_entries> for rails, and associates them with signal_name (and optionally with bus_label entries)

```
[Die Supply Pads] signal_name bus_label
  | pad_name
  VDDQ     VDD
  VSSQ     VSS
```
Interconnect Model for Buffer-to-Die Pad Side

[Interconnect Model Set] Full_ISS_PDN

<table>
<thead>
<tr>
<th>Interconnect Model</th>
<th>Partial_ISS_buf_pad</th>
<th>File_IBIS-iss</th>
<th>buf_pad_iss</th>
<th>buf_pad_2_typ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number_of_terminals</td>
<td>= 10</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Pad_I/O pin_name A1 | DQ1 (DQ signal) |
2. Pad_I/O pin_name A2 | DQ2 (DQ signal) |

POWER and GND terminals with pad_names and pin_names

3. Pullup_ref pin_name A1 | VDD (POWER connection) |
4. Pulldown_ref pin_name A1 | VSS (GND connection) |
5. Buffer_I/O pin_name A1 | DQ1 (DQ signal) |
6. Pullup_ref pin_name A2 | VDD (POWER connection) |
7. Pulldown_ref pin_name A2 | VSS (GND connection) |
8. Buffer_I/O pin_name A2 | DQ2 (DQ signal) |

POWER and GND terminals with signal_names

9. Pad_Rail pad_name VDDQ | VDD POWER |
10. Pad_Rail pad_name VSSQ | VSS GND |

[End Interconnect Model]
[Interconnect Model] for Buffer-to-Die Pad Side (Expanded)

[Interconnect Model Set] Full_ISS_PDN

[Interconnect Model] Partial_ISS_buf_pad

File_IBIS-ISS    buf_pad.iss    buf_pad_2_typ

Number_of_terminals = 10

1  Pad_I/O    pin_name  A1 |  DQ1 (DQ signal)
2  Pad_I/O    pin_name  A2 |  DQ2 (DQ signal)

POWER and GND terminals with pad_names and pin_names
3  Pullup_ref  pin_name  A1 |  VDD (POWER connection)
4  Pulldown_ref pin_name  A1 |  VSS (GND connection)
5  Buffer_I/O  pin_name  A1 |  DQ1 (DQ signal)
6  Pullup_ref  pin_name  A2 |  VDD (POWER connection)
7  Pulldown_ref pin_name  A2 |  VSS (GND connection)
8  Buffer_I/O  pin_name  A2 |  DQ2 (DQ signal)

POWER and GND terminals with signal_names
9  Pad_Rail    pad_name  VDDQ |  VDD  POWER
10 Pad_Rail    pad_name  VSSQ |  VSS  GND

[End Interconnect Model]
[Interconnect Model] for Die Pad-to-Pin Side

Buffer
Terminals

Die
Pad
Terminals

Pins

C1 VDD POWER
A1 DQ1 DATA_MODEL
C2 VSS GND
A2 DQ2 DATA_MODEL

[Interconnect Model] Partial_ISS_pad_pin_2
| File_IBIS-ISS      pad_pin.iss      pad_pin_2_typ
| Number_of_terminals = 8
| 1 Pin_I/O pin_name A1 | DQ1 (DQ signal)
| 2 Pin_I/O pin_name A2 | DQ2 (DQ signal)
| 3 Pin_Rail signal_name VDD | VDD (POWER connection)
| 4 Pin_Rail signal_name VSS | VSS (GND connection)
| 5 Pad_I/O pin_name A1 | DQ1 (DQ signal)
| 6 Pad_I/O pin_name A2 | DQ2 (DQ signal)
| 7 Pad_Rail pad_name VDDQ | pad_name with VDD
| 8 Pad_Rail pad_name VSSQ | pad_name with VSS

[End Interconnect Model]

[End Interconnect Model Set]
[Interconnect Model] for Die Pad-to-Pin Side (Expanded)

[Interconnect Model]

File and subcircuit

<Terminal lines> for connecting the subcircuit nodes (by position) to the interconnect structure

[Interconnect Model] Partial_ISS_pad_pin_2

| File_IBIS-ISS                   pad_pin.iss  pad_pin_2_typ |
|-------------------------------|-----------------|
| Number_of_terminals = 8       |                 |
| 1 Pin_I/O pin_name A1 | DQ1 (DQ signal) |
| 2 Pin_I/O pin_name A2 | DQ2 (DQ signal) |
|                             |                 |
| POWER and GND terminals with signal_names |
| 3 Pin_Rail signal_name VDD | VDD (POWER connection) |
| 4 Pin_Rail signal_name VSS | VSS (GND connection) |
| 5 Pad_I/O pin_name A1 | DQ1 (DQ signal) |
| 6 Pad_I/O pin_name A2 | DQ2 (DQ signal) |
|                             |                 |
| POWER and GND terminals with pad_names |
| 7 Pad_Rail pad_name VDDQ | pad_name with VDD |
| 8 Pad_Rail pad_name VSSQ | pad_name with VSS |

[End Interconnect Model]

[End Interconnect Model Set]
Complete [Interconnect Model Set] With Both [Interconnect Model]s

[Interconnect Model Set] Full_ISS_PDN
[Interconnect Model] Partial_ISS_buf_pad
File_IBIS-ISS buf_pad.iss buf_pad_2_typ
Number_of_terminals = 10
1. Pad_I/O pin_name A1 | DQ1 (DQ signal)
2. Pad_I/O pin_name A2 | DQ2 (DQ signal)
| POWER and GND terminals with pin_names
3. Pullup_ref pin_name A1 | VDD (POWER connection)
4. Pulldown_ref pin_name A1 | VSS (GND connection)
5. Buffer_I/O pin_name A1 | DQ1 (DQ signal)
6. Pullup_ref pin_name A2 | VDD (POWER connection)
7. Pulldown_ref pin_name A2 | VSS (GND connection)
8. Buffer_I/O pin_name A2 | DQ2 (DQ signal)
| POWER and GND terminals with signal_names
9. Pad_Rail signal_name VDDQ | VDD POWER
10. Pad_Rail signal_name VSSQ | VSS GND

[Interconnect Model] Partial_ISS_pad_pin_2
File_IBIS-ISS pad_pin.iss pad_pin_2_typ
Number_of_terminals = 8
1. Pin_I/O pin_name A1 | DQ1 (DQ signal)
2. Pin_I/O pin_name A2 | DQ2 (DQ signal)
| POWER and GND terminals with signal_names
3. Pin_Rail signal_name VDD | VDD (POWER connection)
4. Pin_Rail signal_name VSS | VSS (GND connection)
5. Pad_I/O pin_name A1 | DQ1 (DQ signal)
6. Pad_I/O pin_name A2 | DQ2 (DQ signal)
| POWER and GND terminals with pad_names
7. Pad_Rail pad_name VDDQ | VDD is signal name
8. Pad_Rail pad_name VSSQ | VSS is signal name

[End Interconnect Model]
[End Interconnect Model Set]

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[Interconnect Model Set Group] (New) for a Selected Group

[Interconnect Model Set Group]   A1_A2_PDN

| Interconnect Model Set Name   File_reference
| Full_ISS_PDN                  NA

[End Interconnect Model Set Group]

[Interconnect Model Set Group] is at same level as [Package Model] for selected group of Buffer_IO pin(s)

Name should be descriptive for easy selection (e.g., A1-A2_PDN)

Can contain several references to [Interconnect Model Set]s

Sets can be in the .ibs file (NA) or in a separate directories

[Interconnect Model]s within a Group must be connected
File_TS, File_TS0 (New) Issue

- Touchstone files can now be documented with a single reference (File_TS) or ground “Node 0” reference (File_TS0)
  - Offering both choices eliminates issue about which is better
  - File_TS0 would not be used for power-aware simulations

- File_IBIS-ISS with S model can be used for more references, if needed
Touchstone Unused Port Termination

- Not an issue with IBIS-ISS – all terminal connections are required
- For Touchstone files
  - `Unused_port_termination <Open | Reference>`
  - Reference: reference impedance reduces the number of Touchstone ports through matrix reduction
  - Open: represents the physically disconnected port
  - EDA tools might still provide an interface to override the choices
- Other options still being discussed
Summary

- BIRD189.x improves IBIS package modeling
- Links IBIS, IBIS-ISS and Touchstone for package models
  - Adds flexible support for package loss, crosstalk and partitioning
- Formalizes and separates Die pads and Buffers
- Other extensions (not covered here) included

New advanced Interconnect format for IBIS Version 7.0!