Concerns when applying Channel Simulation to DDR4 Interface

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Agenda

- Background
- About Channel Simulation
- Investigate LTI system of DDR4 Signal
- Summary
Background
Background

- DDR4 SDRAM JEDEC STANDARD: At BER=1e-16, the Eye Margin is necessary.
- Simulation of a great many bits is necessary to get a highly precise 1e-16 BER Contour.
- The conventional SPICE simulation takes time.
- Therefore high-speed Channel simulation using IBIS-AMI is necessary.
- In Channel simulation, the analog channel (include Driver, Receiver, Transmission line) must be LTI (Linear time-invariant) system.
- Therefore investigated whether DDR4 DQ Signal was LTI system this time.

Eye Mask

1e-16 BER Contour

DDR4-1866 Write direction DQ Eye Diagram
About Channel Simulation
Channel Simulation Method

Ideal Unit Step Signal

Analog Channel
[Linear Time-Invariant (LTI) system]

Step Response

\[ u(t) \]

\[ 1 \]

\[ 0 \rightarrow t \]

\[ t \]

\[ s(t) \]

\[ 0 \rightarrow t \]

**Time Derivative**

\[ h(t) = \frac{ds(t)}{dt} \]

**Impulse Response**

\[ h(t) \]

\[ 0 \rightarrow t \]

**Convolution**

**Eye Diagram**

**TX Input Bit Stream**
Linear Time-Invariant (LTI)

LTI System

Input(t) \Rightarrow Output(t)

2Input(t) \Rightarrow 2Output(t)

Input(t) \Rightarrow Output(t)

Linear

Time-Invariant

Input(t-T) \Rightarrow Output(t-T)
Linear Time-Invariant (LTI)

Transmitter IBIS-AMI

SERDES topology using IBIS-AMI

Receiver IBIS-AMI

- Up Impulse response matches Down Impulse response.
- Therefore the analog channel characteristic is able to show by one Impulse response.
- And it is the LTI system.

Reverse Dn for a comparison

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Is the DQ Signal of DDR4 LTI?

- The resistance value of Rout and ODT is shown in the IBIS model name.
  → Is it good to treat DDR4 DQ Signal as LTI system like SERDES?
- Investigated whether DDR4 DQ Signal was LTI system.
Investigate LTI system of DDR4 Signal
Investigated DDR4 Signals

<table>
<thead>
<tr>
<th>Case</th>
<th>Mbps</th>
<th>Investigated DDR4 Signal</th>
<th>Result</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>1866</td>
<td>DDR4 Signal No.1</td>
<td>Write</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Attached</td>
</tr>
<tr>
<td>2</td>
<td>2133</td>
<td>DDR4 Signal No.2</td>
<td>Write</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Attached</td>
</tr>
<tr>
<td>3</td>
<td>2133</td>
<td>DDR4 Signal No.3</td>
<td>Write</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>Attached</td>
</tr>
<tr>
<td>4</td>
<td>2133</td>
<td>DDR4 Signal No.4</td>
<td>Write</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Attached</td>
</tr>
</tbody>
</table>

- Used Max model of IBIS in the Spice simulation and the Channel simulation.
- Example of the investigated topology

Controller → VIA → VIA → DDR4
Investigation method

- Confirm the Impulse responses of rising step signal and falling step signal.
  → Are two impulse responses same?

- Comparison between the Spice simulation and the Channel simulation.
  → Is the Channel simulation same as the Spice simulation?

- Use the Impulse response by rising step signal.
  (=Impulse_up_response)
[Case1] DDR4 Signal No.1 Write

- Impulse response: up ≒ down
- Eye diagram: Spice ≒ Channel
[Case3] DDR4 Signal No.2 Write

- Impulse response: up ≠ down
- Eye diagram: Spice ≠ Channel
Why is it “Eye diagram: Spice≠Channel”? Checked IBIS.

Rising and Falling Waveform of Controller (Driver) The start of the change are greatly different.

Made the start of the change the same experimentally.

The cause is difference between rise timing and fall timing of the driver.
[Case8] DDR4 Signal No.4 Read

- Impulse response: up ≠ down
- Eye diagram: Spice ≠ Channel
Why is “Eye diagram: Spice≠Channel”? Checked IBIS.

Composition of [Power clamp], [GND clamp] and [Submodel] of the Controller (Receiver). It is nonlinear.

Reflection from L to H (Up) ≠ Reflection from H to L (Down). Therefore the Impulse responses are different in “Up” and “Down”. Used the Up Impulse response in the Channel simulation.

The cause is that the ODT of Receiver is Nonlinear. (The value of ODT is different in “Up” and “Down”.)
## Investigation Results

<table>
<thead>
<tr>
<th>Case</th>
<th>Investigated DDR4 Signal</th>
<th>Impulse up=down?</th>
<th>Eye diagram Spice=Channel?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DDR4 Signal No.1</td>
<td>Write close</td>
<td>close</td>
</tr>
<tr>
<td>2</td>
<td>DDR4 Signal No.1</td>
<td>Read same</td>
<td>close</td>
</tr>
<tr>
<td>3</td>
<td>DDR4 Signal No.2</td>
<td>Write different</td>
<td>different</td>
</tr>
<tr>
<td>4</td>
<td>DDR4 Signal No.2</td>
<td>Read close</td>
<td>close</td>
</tr>
<tr>
<td>5</td>
<td>DDR4 Signal No.3</td>
<td>Write close</td>
<td>same</td>
</tr>
<tr>
<td>6</td>
<td>DDR4 Signal No.3</td>
<td>Read close</td>
<td>same</td>
</tr>
<tr>
<td>7</td>
<td>DDR4 Signal No.4</td>
<td>Write close</td>
<td>close</td>
</tr>
<tr>
<td>8</td>
<td>_DDR4 Signal No.4</td>
<td>Read different</td>
<td>different</td>
</tr>
</tbody>
</table>
Summary
Investigated whether DDR4 DQ Signal was LTI system.
Most of the cases investigated were LTI system.
However, there were two cases that were not LTI (NLTV: Non Linear Time Variant).
The reasons why they are not LTI system are as follows.
1. Driver IBIS: There is a difference at the start time of the Rise and the Fall of Waveform.
2. Receiver IBIS: ODT (Composition of [Power clamp], [GND clamp] and [Submodel]) is Nonlinear.
From the above, it is necessary to consider that there are not only LTI but also nonlinear systems (NLTV) in the DDR4 signal.
Is IO of DDR5 LTI?
References

  http://www.ibis.org/ver6.1/ for IBIS 6.1

- JEDEC STANDARD DDR4 SDRAM JESD79-4A
  Revision of JESD79-4, September 2012 for DDR4 Standard